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Parallel Concatenation of LDPC Codes with LTE Modulation Schemes

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Abstract: low-density parity checks (LDPC) codes have received significant interest for communication system applications for their performance as error correction codes. LDPC codes outperform parallel turbo codes, which are based on a convolutional encoder. This paper proposes parallel concatenation of LDPC codes of small length. The proposed method employs a summation of the estimation output technique from the LDPC decoder. The study performed simulations to evaluate the parallel concatenation of two and three irregular LDPC codes at code rates of 1/2 and 1/3. The simulations evaluated a low number of iterations about ten only for each decoder. We further compare the bit error rate performance of different cases with an additive white Gaussian noise channel in consideration of the quadrature phase shift keying, 16-quadrature amplitude modulation and 64-quadrature amplitude modulation schemes. The study is focused on such modulation schemes related to their modern application as standard modulation types used with long - term evolution.The simulation results clearly demonstrated the improved system performance with each modulation scheme.

Keywords: 16-QAM, 64-QAM, AWGN, LDPC, Parallel concatenated code, QPSK

1 Introduction

The widely known low-density parity check (LDPC) is an error correction code, firstly introduced by Gallager in 1962 [1] and rediscovered by MacKay and Neal in 1996. This class of code exhibits near-ideal performance. The LDPC codes are linear block codes constructed using a sparse matrix H in a binary case and are distinguished by relatively few 1s among many 0s. The LDPC decoder employs an iterative decoding algorithm; however, this algorithm is unable to encompass the computing capabilities of the processors available at that time [1]. Resultantly, LDPC codes were forgotten until 1996 inspite of significant attempts by Tanner in 1981 [2] to rediscover the LDPC. The number of iterations influence the iterative decoding process.The greater numbers of iterations have significantly improved the decoding performance.

The regular LDPC codes include a fixed number of 1s per row and column in the initial construction of regular parity check matrix H, with the number of 1s being significantly less than the number of 0s. LDPC codes are constructed using sparse binary matrix H and referred to as regular LDPC codes. The number of 1s in both rows and columns needs to be small compared to the code length. In addition, LDPC codes can be implemented as random.The structured LDPC codes are used to construct the sparse parity check matrix H relative to the method. In general, random LDPC codes demonstrate better bit error rate (BER) performance as compared to structured LDPC codes [8]. However, the number of 1s per row and column can be varied to construct another type of parity check matrix H, i.e., irregular LDPC codes. In general, many studies have concluded out performance of irregular LDPC codes as compared to regular LDPC codes in terms of BER performance [1]. These studies have proposed several methods for the construction of irregular LDPC codes [3]. The two primary methods represent LDPC codes i.e., using a matrix to describe both the parity and generator matrix of the code and a graphical method (i.e., the Tanner graph). The Tanner graph provides a representation of an LDPC code by connecting two types of nodes, i.e., variable nodes and check nodes. An example parity matrix H for an LDPC code (8,4) can be

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expressed as follows.

$$H = \begin{vmatrix} 0\,1\,0\,1\,1\,0\,0\,1 \\ 1\,1\,1\,0\,0\,1\,0\,0 \\ 0\,0\,1\,0\,0\,1\,1\,1 \\ 1\,0\,0\,1\,1\,0\,1\,0 \end{vmatrix} \quad (1)$$

Here the columns represent variable nodes and the rows represent check nodes. The Tanner graph draws connection lines between variable nodes and check nodes at locations where hi,j represent element in H is 1. Fig. 1 shows a Tanner graph. In Fig. 1, the bold lines connect

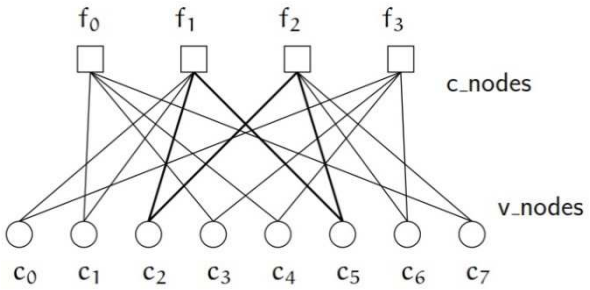

Fig. 1: Tanner graph of the parity checks matrix H in Eq. (1) [1]

nodes c2, c5, f1, and f2. These lines form a closed loop and need to be avoided to design an effective LDPC code. The large LDPC code parity check matrix H avoids such closed loops in practice. These closed loops lock the decoding process in an infinite loop and prevent an erroneous message from being decoded. This is particular for the hard-decision decoding algorithm.

2 Hard Decision Decoding Algorithm

The hard decision algorithm depends on message passing. This algorithm is described as follows.An input message is first passed to variable nodes in a Tanner graph.The message bits are passed to check nodes according to the connections in the Tanner graph.The check nodes receive multiple bits from each variable node. Then, the algorithm performs a parity check. If the result is 0, the bits are sent to variable nodes without change; otherwise, the check process inverts or flips the bit value and sends the bits to a variable node.Check nodes collect the vote result of the bit value. If the number of 1s is greater than the number of 0s, the decoded bit equals 1; otherwise, it equals 0.If all bits are free of error, the loop is closed; otherwise, variable nodes resend the bits to check nodes until the number of iterations finished. We present numerical examples to explain the process and declare all notes.Example 1: for the parity check matrix H in Eq. (1) with the error-free code word [1 0 0 1 0 1 0 1], if the algorithm inserts a single bit error at position C6, the received message will be [1 0 0 1 0 1 1 1]. The algorithm is described in Table 1.

For a check node, if the number of 1s is even in the received row, then the check returns 0 and the received bits are sent back to variable nodes; otherwise, if the check returns 1, bits are flipped and resent to variable nodes. The variable nodes use a simple vote mechanism after receiving bits from the check nodesto determine the correction bit by taking the originally received bits and the bits received from the check point as an input. Herein,two back branches and the original bit comprise the three bits used to make the hard decision. This process is described in Table 2.

According to the C6 row (shown in bold) in Table 2.,the message is corrected effectively because the vote shows two 0s compared to a single 1; thus, the hard decision sets the C6 position bit value to 1. Therefore, after all the received code word with erroneous bit at C6 right corrected after decoding process.The error positions are sensitive in a poorly-designed LDPC code with a closed cycle. Therefore, real LDPC codes are typically large and are generated using an accurate construction algorithm. In the simple Tanner graph shown in Fig. 1, there is a closed cycle (bold lines) from nodes C2 f1 C5 f2 C2 [*2]. We examine another example and show the flow of the hard decision algorithms calculations to illustrate this point.

Example 2: for the received single error bit (shown in bold) at location C2, the code word is [1 0 1 1 0 1 0 1], the same calculations from Example 1 are performed and the results are shown in Table 3.

Here in, the error at node C2 (shown in bold) is corrected, However, another error appears in the closed loop cycle at C5, i.e., the original correct bit (value 1) is converted to an erroneous bit (value 0). Therefore, we examine the calculations of the iterative hard-decision algorithm, starting with a new code word with an error at position C5, i.e., [1 0 0 1 0 0 0 1].

Here in, the error at position C5 is corrected. However, the same error appears at position C2. Resultant, this calculation cannot correct such an error.

The most common algorithms include LDPC decoding algorithms, the belief propagation algorithm (BPA), the message passing algorithm, and the sum product algorithm. The soft decision algorithm generally yields better decoding results [*1].

2.1 LDPC APPLICATION

The competition exists between turbo codes and LDPC codes. Turbo codes are typically employed in communication applications as they are well known and demonstrate good error correction code performance. The LDPC codes are also applied in practical applications. Because, many communication applications require

Table 1: Message passing hard decision LDPC decoder algorithm (EXAMPLE 1)

Check nodes	Received/sent					Check
f0	Received	C1=0	C3=1	C4=0	C7=1	0
	Sent	0=C1	1=C3	0=C4	1=C7	
f1	Received	C0=1	C1=0	C2=0	C5=1	0
	Sent	1=C0	0=C1	0=C2	1=C5	
f2	Received	C2=0	C5=1	C6=1	C7=1	1
	Sent	1=C2	0=C5	0=C6	0=C7	
f3	Received	C0=1	C3=1	C4=0	C6=1	1
	Sent	0=C0	0=C3	1=C4	0=C6	

Table 2: Message vote hard decision LDPC decoder (EXAMPLE 1)

Variable node	Received	Message from check nodes	# of 1s	# of 0s	Result
C0	1	$f1=1\ f3=0$	2	1	1
C1	0	$f0=0\ f1=0$	0	3	0
C2	0	$f1=0\ f2=1$	1	2	0
C3	1	$f0=1\ f3=0$	2	1	1
C4	0	$f0=0\ f3=1$	1	2	0
C5	1	$f1=1\ f2=0$	2	1	1
C6	1	$f2=0\ f3=0$	1	2	0
C7	1	$f0=1\ f2=0$	2	1	1

Table 3: Message passing hard decision LDPC decoder algorithm (EXAMPLE 2)

Check nodes	Received/sent				Check
f0	Received	$C3=1$	$C4=0$	$C7=1$	0
	Sent	$1=C3$	$0=C4$	$1=C7$	
f1	Received	$C1=0$	$C2=1$	$C5=1$	1
	Sent	$1=C1$	$0=C2$	$0=C5$	
f2	Received	$C5=1$	$C6=0$	$C7=1$	1
	Sent	$0=C5$	$1=C6$	$0=C7$	
f3	Received	$C3=1$	$C4=0$	$C6=0$	0
	Sent	$1=C3$	$0=C4$	$0=C6$	

Table 4: Message vote Hard decision LDPC decoder, show error at location C2 (EXAMPLE 2)

Variable node	Received	Message from check nodes	# of 1s	# of 0s	Result
C0	1	$f1=0\ f3=1$	2	1	1
C1	0	$f0=0\ f1=1$	1	2	0
C2	1	$f1=0\ f2=0$	1	2	0
C3	1	$f0=1\ f3=1$	3	0	1
C4	0	$f0=0\ f3=0$	0	3	0
C5	1	$f1=0\ f2=0$	1	2	0
C6	0	$f2=1\ f3=0$	1	2	0
C7	1	$f0=1\ f2=0$	2	1	1

Table 5: Message passing hard decision decoder algorithm

Check nodes	Received/sent					Check
f0	Received	$C1=0$	$C3=1$	$C4=0$	$C7=1$	0
	Sent	$0=C1$	$1=C3$	$0=C4$	$1=C7$	
f1	Received	$C0=1$	$C1=0$	$C2=0$	$C5=0$	1
	Sent	$0=C0$	$1=C1$	$1=C2$	$1=C5$	
f2	Received	$C2=0$	$C5=0$	$C6=0$	$C7=1$	1
	Sent	$1=C2$	$1=C5$	$1=C6$	$0=C7$	
f3	Received	$C0=1$	$C3=1$	$C4=0$	$C6=0$	0
	Sent	$1=C0$	$1=C3$	$0=C4$	$0=C6$	

Table 6: Message vote hard decision LDPC decoder

Variable node	Received	Message from check nodes	# of 1s	# of 0s	Result
C0	1	$f1=0$ $f3=1$	2	1	1
C1	0	$f0=0$ $f1=0$	1	2	0
C2	0	$f1=0$ $f2=0$	1	2	0
C3	1	$f0=1$ $f3=1$	3	0	1
C4	0	$f0=0$ $f3=0$	0	3	0
C5	0	$f1=0$ $f2=0$	1	2	0
C6	0	$f2=1$ $f3=0$	1	2	0
C7	1	$f0=1$ $f2=0$	2	1	1

Table 7: Generated irregular LDPC codes

Code rate	Code type
1/2	Cb (96, 48)
	Cb (144, 72)
	Cb (192, 96)
	Cb (240, 120)
1/3	Cb (144, 48)
	Cb (216, 72)
	Cb (288, 96)
	Cb (360, 120)

excellent BER performance such as deep space communication systems. However, there are other metrics used to evaluate the performance of turbo and LDPC codes other than BER. The factors like complexity of a systems encoders and decoders are also used to evaluate these codes. The consideration of decoding time as a performance measure leads the comparison in favor of LDPC codes. They present the low complexity and flexibility relative to the desired code rate for the given application [3].

The several important applications require high BER performance such as deep space communication systems. These systems require an extremely low BER. The concatenation approach is appropriate to achieve low BERs between an LDPC code as an outer system encoder and a turbo code as an inner system encoder. The overall system can exploit the advantages of both codes in such serially-concatenated codes. The both LDPC and turbo codes can be applied in a practical decoder design, using the Bahl-Cocke-Jelinek-RavivBCJR algorithm. The previous study has advocated for design of an efficient hardware architecture with high resource reuse [4] using such concatenated codes.

The turbo code represents a standard error correction code in the long term evolution of LTE systems. The hardware implementations for system encoders and decoders are employed in field-programmable gate arrays (FPGA) [5].The LDPC codes are implemented using the

Table 8: Results for two parallel LDPC codes rate 1/2

Modulation	LDPC Cb(n, k)Rate 1/2	SNR dB	BER
QPSK	Cb (96, 48)	2	0.00044399
	Cb (144, 72)	2	0.000164
	Cb (192, 96)	2	9.89910^{-5}
	Cb (240, 120)	2	4.499610^{-5}
16-QAM	Cb (96, 48)	9	0.00015999
	Cb (144, 72)	9	2.610^{-5}
	Cb (192, 96)	9	5.999810^{-6}
	Cb (240, 120)	9	2.999810^{-6}
64-QAM	Cb (96, 48)	12	0.0037649
	Cb (144, 72)	12	0.001757
	Cb (192, 96)	12	0.0016859
	Cb (240, 120)	12	0.0014269

Table 9: Results for two parallel LDPC codes rate 1/3

Modulation	LDPC Cb(n, k)Rate 1/2	SNR dB	BER
QPSK	Cb (144, 48)	1.2	8.799710^{-5}
	Cb (216, 72)	1.2	210^{-6}
	Cb (288, 96)	1.2	1.299910^{-6}
	Cb (360, 120)	1.1	9.999210^{-7}
16-QAM	Cb (144, 48)	7	5.999810^{-6}
	Cb (216, 72)	6	7.699910^{-5}
	Cb (288, 96)	7	9.999710^{-7}
	Cb (360, 120)	7	9.999210^{-7}
64-QAM	Cb (144, 48)	12	8.999710^{-6}
	Cb (216, 72)	11	1.110^{-5}
	Cb (288, 96)	11	2.999910^{-6}
	Cb (360, 120)	11	9.999210^{-6}

Table 10: Results for three parallel LDPC codes rate 1/2

Modulation	LDPC Cb(n, k)Rate 1/2	SNR dB	BER
QPSK	Cb (96, 48)	2	0.0004439
	Cb (144, 72)	2	0.000164
	Cb (192, 96)	2	9.899710^{-5}
	Cb (240, 120)	2	4.499610^{-5}
16-QAM	Cb (96, 48)	9	1.799910^{-5}
	Cb (144, 72)	8	6.799910^{-5}
	Cb (192, 96)	8	2.199810^{-5}
	Cb (240, 120)	8	1.799910^{-5}
64-QAM	Cb (96, 48)	12	0.00139
	Cb (144, 72)	12	0.000582
	Cb (192, 96)	12	0.00043899
	Cb (240, 120)	12	0.00036497

Table 11: Results for three parallel LDPC codes rate 1/3

Modulation	LDPC Cb(n, k)Rate 1/3	SNR dB	BER
QPSK	Cb (144, 48)	1.2	3.999910^{-6}
	Cb (216, 72)	0.6	310^{-6}
	Cb (288, 96)	0.5	3.49910^{-6}
	Cb (360, 120)	0.5	9.999210^{-7}
16-QAM	Cb (144, 48)	6	2.199910^{-5}
	Cb (216, 72)	6	9.999910^{-6}
	Cb (288, 96)	6	9.999210^{-7}
	Cb (360, 120)	6	9.999710^{-7}
64-QAM	Cb (144, 48)	11	$7.999710 - 6$
	Cb (216, 72)	11	$310 - 6$
	Cb (288, 96)	10	$5.999710 - 6$
	Cb (360, 120)	10	$3.999710 - 6$

same technology employed in FPGAs. The previous studies have proposed a high-speed parallel LDPC encoder that employs the BPA [6]. This encoder attempts to reduce the iterative decoding process by updating only incorrect bit information in the decoding algorithm.It aims to improve efficiency and reduce the time-delay of the decoder. The LDPC codes are also employed in terahertz applications. The atmospheric absorption, scattering, and scintillation reduce transmission quality [7] in these applications. The soft decision LDPC decoder algorithm has been applied to improve the BER of a system that uses on off keyingOOK modulation. The research [7] proposes a scheme based on the concatenation of non-custom LDPC and turbo codes that present excellent error-correction performance. Moreover, both LDPC and turbo codes are decoded with the BCJR algorithm. The preliminary results suggest to design an efficient hardware architecture with high resource reuse.

The quasi-cyclic LDPC codes are another type of LDPC codes [8]. They are structured codes that provide a very efficient implementation while maintaining excellent performance. The quasi-cyclic codes are characterized by a cyclic shift of one codeword result in another codeword, and are achieved due to the cyclic structure. Quasi-cyclic codes require less memory as compared to conventional LDPC codes. These further demonstrate high-speed decoding due to the sparseness of the parity check matrix [8]. This type of LDPC code is employed as a standard error correction code in wireless communications systems such as IEEE 802.1, IEEE 802.11ac, and IEEE 802.16e. They support high data rates, such as 1/2, 2/3, 3/4, and 5/6.The previous study focused on quasi-cyclic LDPC codes [9], and proposed a coding technique that employs soft decision decoding with an increased number of decoder iterations to achieve better performance. Another study concentrated on low rate quasi cyclic low density parity check code QC-LDPC codes and their application to reconfigurable structures in a space information network [10]. This system achieved a BER of approximately 0.1 dB gain as compared to common QC-LDPC codes.

The previously-proposed visible light system uses LDPC codes as the primary error correction codes [11]. This system uses avalanche photo diodes, which are frequently used in visible light communication systems. A regular LDPC code (3,6) with a block length of 20,000 results in a 0.7-dB gain with an LDPC decoder designed for signal-independent noise. A previously-proposed image transmission application also exploits the benefits of LDPC codes [12]. The unequal error protection in image transmission uses irregular LDPC codes by mapping important image bits to a variable node with higher degrees of irregular LDPC code sand flowed by quadrature amplitude modulation (QAM). This system demonstrates effective unequal error protection performance. As mentioned previously, LDPC codes are frequently used as error correction codes in communication systems. However, one interesting approach has proposed a different use of LDPC codes [*13], wherein a QC-LDPC code parity matrix H is used to construct a measurement matrix for compressed sensing. This system exploits the benefits of the parity check matrix properties rather than a random measurement matrix, which facilitates the implementation of FPGAs for compressed sensing applications.

2.2 Parallel Concatenated LDPC Codes

The performance of LDPC codes as standalone codes is very good, which makes them suitable for improving the performance of communication systems, and parallel concatenation of LDPC codes offers good performance relative to channel effects. The previously-proposed communication system has employed the parallel concatenation of multiple LDPC codes [4]. Here, the

decoder process on the receiver side uses a code word selector. The system receiver is shown in Fig. 2. This system employs an iterative BPA and depends on predefined equivalent parity check matrices that do not change during the decoding process.

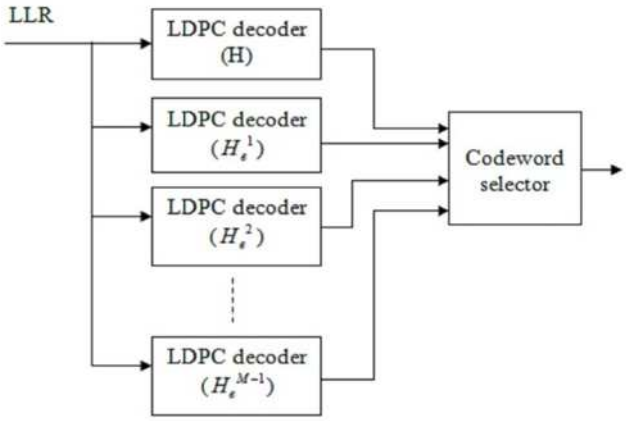

Fig. 2: Parallel concatenated LDPC code decoder [4]

The system shown in Fig. 2 depends on the operation of the codeword selector, which selects invalid codewords with the fewest errors [4]. This system uses code rates of R = 1/2, R = 2/3, and R = 3/4with large code lengths,n (e.g., 1944 and2304 bits). The results of this system show improvement as compared to a conventional LDPC code decoder (approximately 0.1 dB at a BER of 10^{-6} [4]).

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2.3 PROPOSED PARALLEL CONCATENATION OF TWO LDPC CODES

The first proposed system for parallel concatenation of LDPC codes comprises two identical irregular LDPC codes. Here in two code rates (i.e., R = 1/2 and 1/3) for irregular LDPC codes are generated. Two parallel concatenated LDPC codes of the same rate are generated for the each case. The simulation considers two LDPC codes wherein R =1/2 in order to design an appropriate system decoder. Then, the codes are replaced by LDPC codes wherein R = 1/3. The proposed system is shown in Fig. 3.

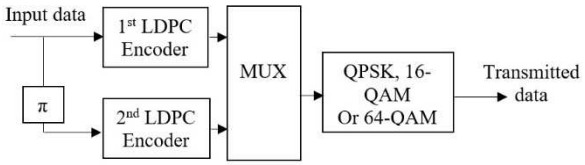

Fig. 3: Encoder for the proposed parallel concatenation of two LDPC codes

Herein, the data flow is input to each irregular LDPC code. Then, a common encoding process produces two code words, i.e., a sequence code word and an interleaved code word, where it represents a random interleaver (Fig. 3). These code words are then multiplexed to construct a frame that is input to one of the LTE modulation schemes, i.e., quadrature phase shift keying (QPSK), 16-QAM, or 64-QAM. In this case, the channel effect is represented by an additive white Gaussian noise. A reciprocal operation is performed on the receiver side, as shown in Fig.4. The

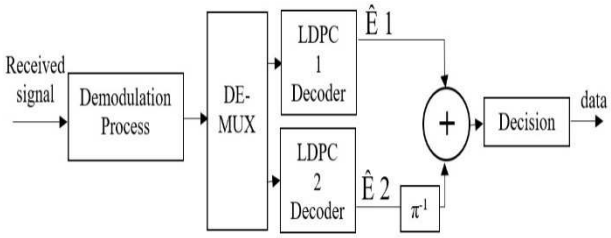

Fig. 4: Decoder for the proposed parallel concatenation of two LDPC codes

receiver side starts with a demodulation process, which uses a demodulator of the same modulation type used on the transmitter side. The received sequence is passed after demodulation to a demultiplexer. The DE-multiplexer redirects the demodulated sequence into two groups for

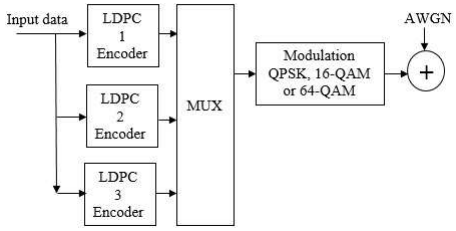

Fig. 5: Parallel concatenation of three LDPC codes as the transmitter encoder

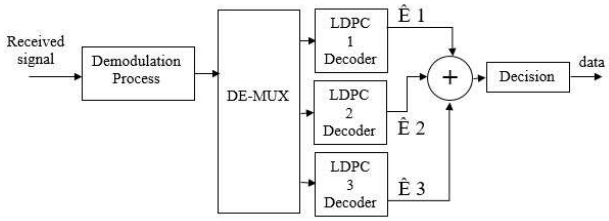

Fig. 6: Decoder for the proposed parallel concatenation of three LDPC codes as the system receiver

each LDPC code decoder. This decoder uses a log likelihood ratio (LLR) algorithm [5], which yields a binary output or provides an estimation regarding the output decoded sequence. The decoding algorithm estimates the output in the proposed system decoder. Importantly, this operation is performs separately for each LDPC decoder. The proposed system then performed summation of the first decoder output and the deinterleaver estimation of the second decoder, where 1 on the receiver side represents the deinterleaver. This operation enlarges the overall decoding estimation to improved estimation of the decoded code word prior to reaching the decision stage. The decoding process for each decoder is iterative, and the final estimation is reached after a specific number of iterations. The simulation results and other system parameters are discussed in Section 7. The LLR decoding algorithm is described as follows [5]. The input to the LDPC decoder is the LLR L(ci), which is defined as follows.

$$L(c_i) = \log \frac{Pr?(ci = 0|channeloutput\,for c_i)}{Pr?(c_i = 1|channeloutput\,for c_i)} \quad (2)$$

where c_i is the i-th bit of the transmitted codeword c. There are three key variables in the algorithm, i.e., $L(rji)$, $L(qij)$, and $L(Qi)$. $L(qij)$ is initialized as $L(qij) = L(ci)$. For each iteration, $L(rji)$, $L(qij)$, and $L(Qi)$ are updated using the following equations (3) [5].

$$L(r_{ji}) = 2atanh(\prod_{i' \in V_{ji}} \tanh(0.5xL_{(}q'j))) \quad (3)$$

$$L(q_{ij}) = L(c_i) + \sum_{j' \in C_i} L(r_{j'i}) \quad (4)$$

$$L(Q_i) = L(c_i) + \sum_{j' \in C_i} L(r_{j'i}) \quad (5)$$

3 PROPOSED PARALLEL CONCATENATION OF THREE LDPC CODES

This system uses the same concept but adds another LDPC code; thus, the system comprises three LDPC codes (Fig. 5). As discussed, the three-code system employs a third LDPC code of identical type relative to the proposed concatenation of two parallel LDPC codes, Therefore, all three encoders are of the same type,when using an irregular LDPC code of rate 1/2. Here, the multiplexer multiplexes three code words before passing the resulting sequence to one of the selected LTE modulation schemes (QPSK, 16-QAM, or 64-QAM). Importantly, a random interleaveris employed to reduce the system complexity. The receiver side performs summation of the three decoder estimations rather than two estimations. The transmitter uses three irregular LDPC encoders and improves overall system performance. The proposed receiver with three parallel irregular LDPC codes is shown in Fig. 6.

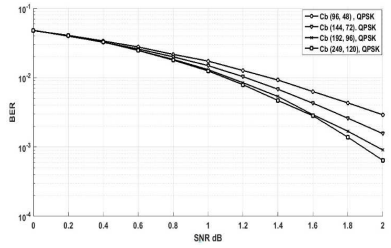

Fig. 7: Parallel concatenation of two LDPC codes (R = 1/2, QPSK)

This strategy yields good overall system performance along with greater system complexity. The previous study [6] has discussed a method to reduce complex LDPC code decoders, such as the large parity check matrices H used in the Digital Video Broadcasting-Satellite-Second Generation system. This method provides both a semi-parallel implementation of the minimum-sum algorithm and synthesis for FPGA prototyping. The system complexity is an interesting point when dealing with LDPC decoders. The large length of LDPC codes leads to improve system BER performance. It also

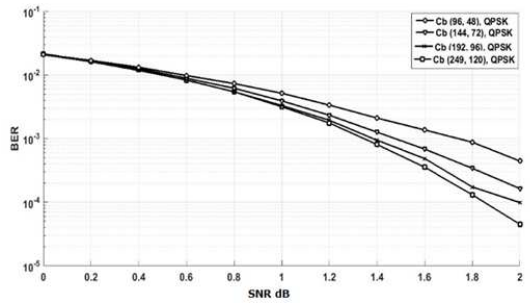

Fig. 8: Three parallel LDPC codes rate 1/2, with QPSK.

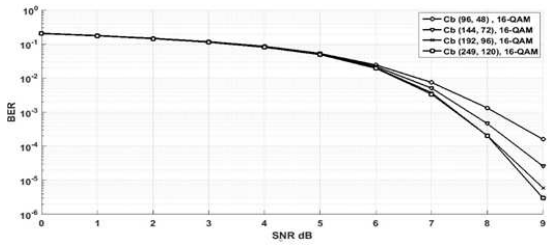

Fig. 9: Parallel concatenation of two LDPC codes (R = 1/2, 16-QAM)

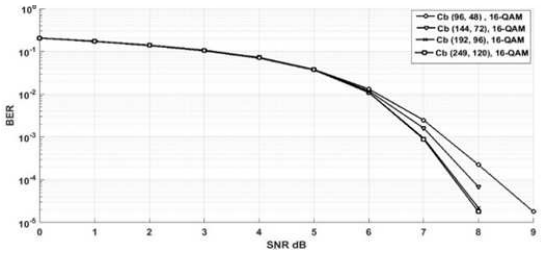

Fig. 10: Parallel concatenation of three LDPC codes (R = 1/2, 16-QAM)

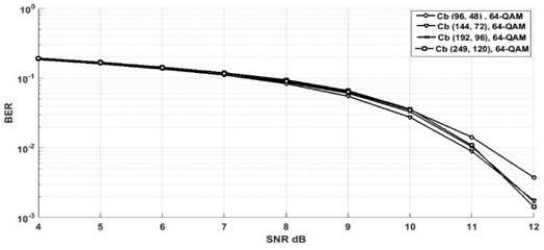

Fig. 11: Parallel concatenation of two LDPC codes (R = 1/2, 64-QAM)

increases system complexity using FPGA to implement system encoder and decoder designed with LDPC codes.

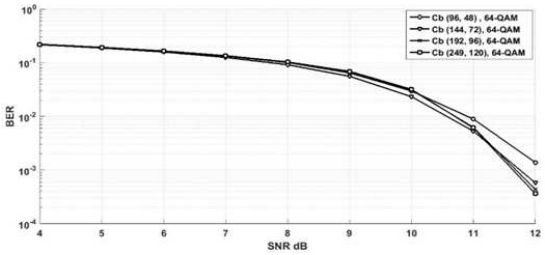

Fig. 12: Parallel concatenation of three LDPC codes (R = 1/2, 64-QAM)

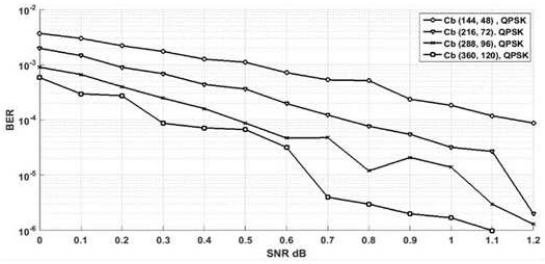

Fig. 13: Parallel concatenation of two LDPC codes (R = 1/3, QPSK)

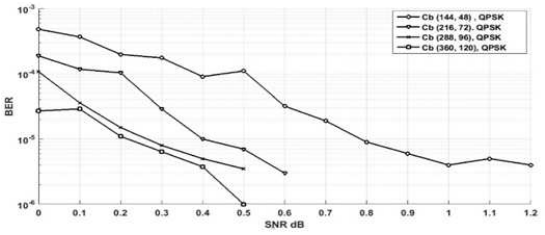

Fig. 14: Parallel concatenation of three LDPC codes (R = 1/3, QPSK)

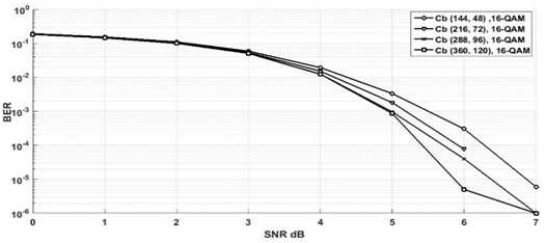

Fig. 15: Parallel concatenation of two LDPC codes (R = 1/3, 16-QAM)

4 SIMULATION RESULTS

The study has conducted simulation tests to evaluate the two proposed systems. The simulations begin by generating two groups of irregular LDPC codes (R = 1/2

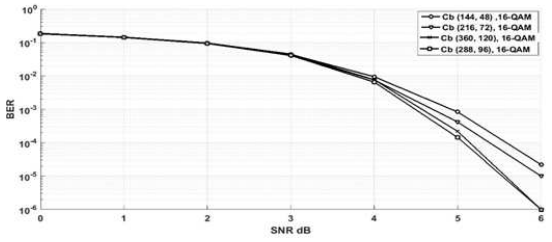

Fig. 16: Parallel concatenation of three LDPC codes (R = 1/3, 16-QAM)

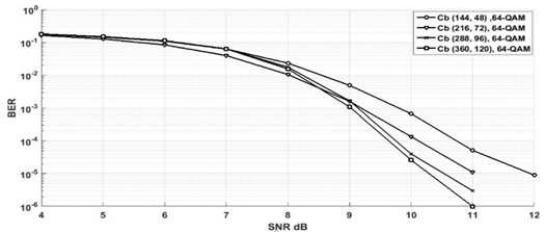

Fig. 17: Parallel concatenation of two LDPC codes (R = 1/3, 64-QAM)

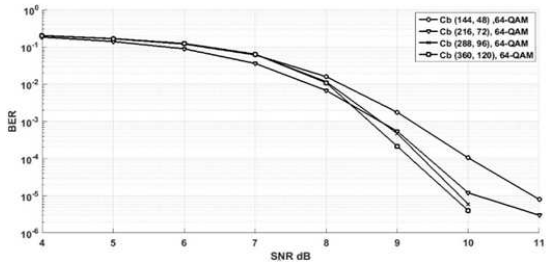

Fig. 18: Parallel concatenation of three LDPC codes (R = 1/3, 64-QAM)

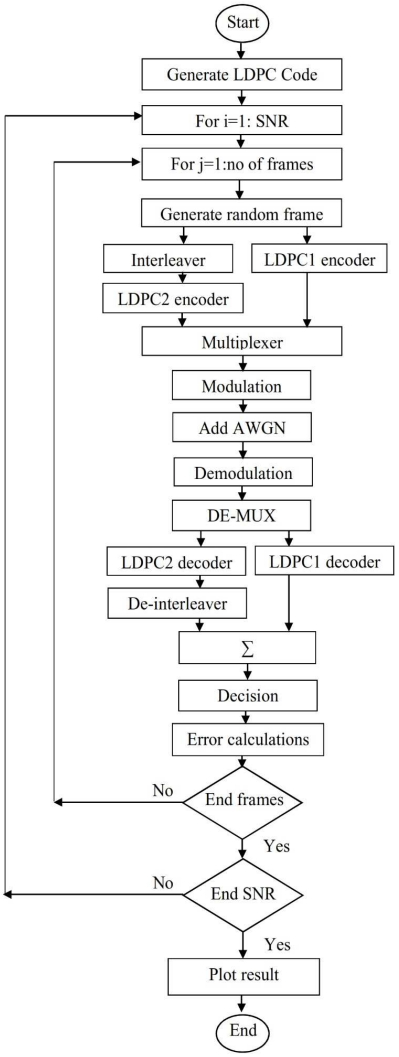

Fig. 19: System Flow Chart (Two Parallel LDPC Codes)

and 1/3). The two groups and their specifications are shown in Table 7.
Here, the code type is specified in the form Cb (n, k), where n and k denote the output code word length and input data length, respectively. The each decoder has its own number of iterations (i.e., 10) because the LLR decoding algorithm is iterative. Thus, the final estimation from each decoder is taken after 10 iterations.

The simulation results obtained for two and three parallel concatenated variable irregular LDPC codes for QPSK, 16-QAM, and 64-QAM with a code rate of R = 1/2 are shown in Figs. 7-12, and Figs. 13-18 show the same with a data rate of R = 1/3. The different results are attributed to the different data rates. QPSK employs a poor signal to achieve a low data rate (2 bits per symbol), 64-QAM employs a high coverage signal to achieve a high data rate (6 bits per symbol), and 16-QAM employs a moderate signal to achieve a data rate of 4 bits per symbol.

5 Perspective

This paper has proposed a method for the parallel concatenation of LDPC codes. The proposed method sums the LDPC decoder estimations rather than using a codeword selector. The proposed method generates two groups of irregular LDPC codes at code rates of R = 1/2

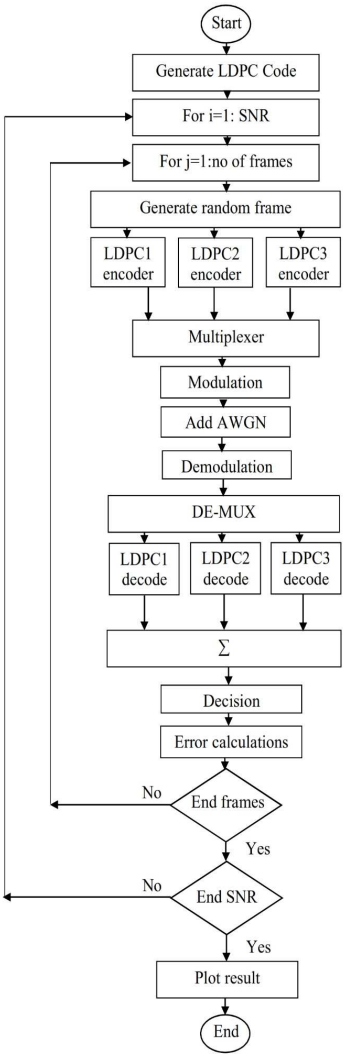

Fig. 20: System Flow Chart (Three Parallel LDPC Codes)

and 1/3 with different code lengths. The simulation results demonstrate overall performance improvement with increasing LDPC code length. The systems are evaluated with two and three parallel LDPC codes using a fixed number of iterations (i.e., 10). The results demonstrate that increasing the number of encoders improves the BER performance of the systems along with increase in system complexity. The simulations include the QPSK, 16-QAM, and 64-QAM schemes and focus on their roles in LTE applications. The simulation results clearly demonstrate improved system performance with each modulation scheme. Importantly, the simulations used the short code lengths as compared to the code lengths employed in practical applications (e.g., DVB). Thus, the selection of LDPC codes length and the number of parallel codes needs to be determined relative to a trade off between system complexity and cost and the target applications BER performance requirements.

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