

An Algorithm for Minimization of Quantum Cost

Anindita Banerjee and Anirban Pathak

Jaypee Institute of Information Technology, Noida, India

Received: October 13, 2009; Accepted April 14, 2010

Published online: 1 January 2012

Abstract: A new algorithm for minimization of quantum cost of classical reversible and quantum circuits have been designed. The quantum cost obtained using the proposed algorithm is compared with the existing results and it is found that the algorithm produces minimum quantum cost in all cases.

Keywords: Quantum cost, circuit optimization and quantum circuit

1. Introduction

According to Landauer's principle [1] any logically irreversible operation on information, is always associated with a loss of energy. For example, each bit of lost information leads to the release of at least $kT \ln 2$ amount of heat. This type of energy loss is expected to become a substantial part of energy dissipation in VLSI circuits in near future. The energy dissipation problem of VLSI circuits can be circumvented by using reversible logic because reversible computation does not require to erase any bit of information. This observation has motivated scientists to design reversible circuits for various purposes [2–28]. If the reversible circuit implements quantum computation and it comprises of quantum gates then it is a quantum circuit and if the reversible circuit implements only classical computation (boolean logic) then it is a classical reversible circuit. In the area of quantum computing several new possibilities appeared which are impossible in classical domain. To be precise, quantum teleportation [14], infinitesimally secured cryptography [15] and super dense coding [16] do not have any classical analogue. All these unique features of quantum communication are associated with some circuits which are reversible in nature. In other words, we require quantum circuits to implement quantum algorithms and protocols. For example, circuits are proposed for implementation of Shor's algorithm [17], quantum teleportation [14], various attacks on quantum key distribution protocols [15, 18], super dense coding [16], quantum error correction [19, 20], fault tolerant quantum computation [21–23], Grover's algorithm [24–26], nondestructive

discrimination of Bell states [27], quantum circuits for addition [28] etc. Here we would like to note that all quantum mechanical operations are reversible and the only difference between a classical reversible gate and a quantum gate is that the classical reversible gate can not handle superposition of states (qubit). Consequently, set of all classical reversible gates form a subset of set of all quantum gates. For example, Cnot gate can be achieved in classical and quantum domains but the Hadamard gate can be achieved in quantum domain only. Therefore, classical reversible circuits are only a subset of quantum circuits and any protocol designed for optimization of particular parameter related to quantum circuits will also be valid for classical reversible circuits.

We have tried to explain the requirement and beauty of quantum circuits and now the question arises: How to obtain these circuits? There exist several algorithms for synthesis of classical reversible circuits [2, 3, 5–7] and quantum circuits [29–31]. But these algorithms do not provide a unique output. For example, a reversible multiplier can be achieved in many ways [8–13]. Therefore, a quantitative measure of the quality of a circuit is required. Some of the important quantitative measures are gate count, number of garbage bits and quantum cost. Gate count is the total number of gates in a circuit, but there is a specific problem with this quantitative measure of circuit quality. Specially it is not unique. If one is allowed to introduce a new gate or a complex gate library then the gate count can be considerably reduced. An n -qubit reversible gate is represented by $2^n \times 2^n$ unitary matrix. Product of any arbitrary number of unitary matrices is always unitary. More-

* Corresponding author: e-mail: anirban.pathak@jiit.ac.in

over serial connection of such gates correspond to multiplication of their matrices and parallel connection corresponds to tensor multiplication of their matrices. Therefore, if we put a set of reversible quantum gates in a black box then it can be visualized as a new gate. Thus the gate count can be reduced to 1. For example in [32] the circuit cost of a full adder circuit from NCT¹ gate library is 4, in [12] it is reduced to 2 by using Peres gate and in [11] it is reduced to 1 by using a new gate. All the differences in circuit cost of full adder is because of choice of non unique gate libraries. Consequently it is important to define an unique gate library for comparison of circuit cost. Further, a good quantum circuit requires minimum number of garbage bits. This is so because garbage bit is defined as an additional output bit, which is required to make a function reversible and it is not used for further computations. The quantum cost² of a reversible circuit [4,33,34,43] is the number of primitive quantum gates needed to implement a circuit. Primitive quantum gates are the elementary building blocks [35,34,36], like Not gate, Cnot gate, controlled- v , controlled- v^+ , rotation gates etc. We can construct Toffoli gate with square root of Not gate (V) and Cnot gate and in that construction the minimum gate count of Toffoli gate is 5 [33] and its quantum cost is also 5. These requirements yield separate measures of quality of a quantum circuit. To be precise, the circuit is better if it has lesser number of garbage bits, circuit cost and quantum cost. But it is often observed that reduction of circuit cost leads to increase in garbage bits and reduction of quantum cost leads to increase in circuit cost [12]. Keeping these in mind, we have recently introduced a new parameter called Total cost (TC) [13], which is the sum of gate count of an optimized circuit, number of garbage bits and quantum cost. For reduction of TC it is required to simultaneously reduce the circuit cost, garbage count and quantum cost. This is an open problem and at present neither an algorithm for simultaneous reduction of all these measures nor a satisfactory algorithm for reduction of quantum cost exists. Before we address the more complex problem of minimization of TC we have to devise a protocol for reduction of quantum cost. In some works [4,6,11,38,43] the quantum cost is calculated straight by adding the quantum cost of respective reversible gates in the circuit or it is optimized by applying deletion rule only. A simple minded systematic approach is also proposed by Maslov *et al.* [36,37]. These facts have motivated us to design an algorithm for minimization of quantum cost and to apply our algorithm to compute quantum cost of different circuits in [4,6,32,36,38,43].

In the next section we have discussed the earlier approaches and their limitations. In section 3, we have proposed an algorithm for calculating the quantum cost of reversible circuits. Here we have also compared our results with the earlier proposals [4,6,32,36,38,43] to establish

¹ NCT gate library is a universal gate library [32] comprising of NOT, Cnot and Toffoli gates.

² Definition of quantum cost is discussed in detail in section 2.

that the quantum cost computed by the proposed algorithm is minimum. Finally we conclude in section 4.

2. Previous works

Cost of an arbitrary unitary gate was first introduced by Barenco *et al.* in 1995 [34]. They had considered all 2×2 gate and Cnot gate as basic gates and had shown that for any 2×2 unitary gate U^3 , we can realize C-U (corresponding controlled U gate) by using at most 6 basic gates. But to analyze the cost of a large gate (n bit Toffoli) he had considered the cost of C-U as $\Theta(1)$. Next year, Smolin and DiVincenzo [33] calculated cost of Fredkin gate. In their calculation they went beyond the definition of Barenco *et al.* and assumed that the cost of every 4×4 gate is 1. This consideration does not have any contradiction with Barenco *et al.*'s definition of cost, as cost of all 2 qubit quantum gates is $\Theta(1)$. Further progress in cost calculation was made by Perkowski *et al.* [39] in 2003, where they show that a one qubit gate costs nothing, if it precedes or follows by a 2 qubit gate. This is so because one qubit gate can be combined with the 2 qubit gate to yield a new two qubit gate. Thus, the cost is calculated as a total sum of 4×4 gates used. Following this definition the cost of swap gate is 1 and that of Peres gate is 4. Peres gate is universal for reversible boolean operations and it has the minimum cost compared to other universal gates. This observation of Perkowski *et al.* had motivated others to use Peres gate to minimize the cost. For example, Maslov and Dueck [40] have used the idea of Perkowski *et al.* and have shown that, the number of elementary quantum operations required to implement Peres gate is less so it can be substituted for n-bit Toffoli network to reduce the cost of n-bit Toffoli gates. Here we would like to note that in the earlier works [33,34,39] quantum cost was mentioned as cost. The term quantum cost was coined by Maslov *et al.* [40,41] in 2003, they have defined quantum cost of a gate G, as the number of elementary quantum operations required to realize the function given by G. Later on, Hung *et al.* [42] had reconsidered the quantum cost estimation protocol defined by Smolin and DiVincenzo [33]. They have stated that each two qubit gate and each symmetric gate pattern (see Fig. 2 of [42]) have quantum implementation cost 1. In essence all these definitions of quantum cost are synonymous and we can follow Perkowski's definition [39] and state that the quantum cost of a classical reversible or quantum circuit is the minimum number of one qubit and two qubit quantum gates needed to implement the circuit.

In recent past quantum cost of different classical reversible and quantum circuits have been reported [3,4,6,11,32,36,38,43]. Simultaneously several efforts have been made to reduce the quantum cost of different

³ n qubit gate is represented by a $2^n \times 2^n$ unitary matrix. Therefore a 2×2 and 4×4 gates correspond to 1 qubit and 2 qubit gates respectively. Different notations have been used in [4,5,39,42,43].

gates/circuits. For example, Barenco *et al.* [34] estimated the cost of a 6 bit Toffoli gate as 61. Maslov and Dueck [40] reduced the quantum cost of this gate initially to 48 by using Peres gate. Further Maslov *et al.* [37] reduced the quantum cost of this gate to 38 by applying local optimization tools. There also exist following two online databases: i) benchmark page of Maslov *et al.* [32] and ii) Revlib [38], which include quantum cost of different circuits. In 2005 Maslov *et al.* [37] have shown that a closer look into the cost metric can classify them into two subclasses: linear cost (where the quantum cost of a circuit is calculated as sum of quantum cost of each gate) and nonlinear cost (where local optimization algorithm is used). According to this classification scheme [37] quantum cost defined in Smolin and DiVincenzo [33] and Hung *et al.* [42] is nonlinear. Interestingly, Mohammadi and Eshghi [4] have given following two prescriptions for calculation of quantum cost:

1. Implement a circuit/gate using only the quantum primitive (2×2) and (4×4) gates and count them.
2. Synthesize the new circuit/gate using the well known gates whose quantum cost is specified and add up their quantum cost to calculate total quantum cost.

In both of these cases we will obtain linear cost metric and consequently the quantum cost obtained in these two procedures may be higher than the actual one unless local optimization algorithms are applied to the entire circuit. When we apply the local optimization algorithm on the entire circuit then we obtain a nonlinear cost metric. The proposed algorithm will calculate nonlinear cost metric. Local optimization is expected to play an important role in minimization of quantum cost. Maslov *et al.* [36,45,46] have realized this fact and have proposed an algorithm for minimization of quantum cost by applying templates and it yields nonlinear cost metric.

Our current work and work of Maslov *et al.*'s [36] is contemporaneous and independent. They differ greatly in their premises, methods and consequences. 1) Maslov *et al.*'s work deal with circuit optimization precisely minimizing gate count by local optimization tools. They have introduced templates and applied them to optimize the gate count. In contrast, our algorithm exploits a conceptual difference between optimization algorithm used for reduction of gate count and the one used for reduction of quantum cost. 2) They are restricted to a particular gate library but to reduce the quantum cost we have introduced new gates as long as the gate is 2×2 or 4×4 quantum gate. 3) In their work the local optimization tools reduces the gate count only, but in our work it is applied to reduce the quantum cost as well. This is shown in Fig. 2c where moving rule [36] (which was essentially designed to reduce circuit complexity) has not reduced the circuit complexity but has reduced the quantum cost. This is evident in the work of Smolin [33]. Further, we would like to note that the quantum cost obtained by Maslov *et al.* is not linear and so is ours. Consequently it will be completely justified to com-

pare the quantum cost obtained by our proposed algorithm with that obtained using Maslov *et al.*'s algorithm.

3. Optimization algorithm

In this section we have proposed an algorithm that optimizes the quantum cost of classical reversible and quantum circuits. It is presented in the form of a flowchart in Fig 1. The flowchart is explained below:

1. The input is a reversible circuit. Here we would like to note that our goal is to find out the minimum number of quantum primitive gates required to implement the circuit and we are not much concerned about the choice of gate library [32,34,35] in principle. But in practice it is easier to work using an input circuit which is constituted using the gates from a standard gate library for which a large/complete set of templates are known. At present there are few set of templates, available for classical reversible circuits [36,46]. However not much templates [36] are reported for quantum circuits and it is not difficult to generate them. Therefore, in the beginning of the algorithm we convert the input reversible circuit into a circuit composed of gates taken from a standard gate library preferably those gate libraries for which a complete/large set of templates are already known.
2. In the next step, we optimize the gate count of the reversible circuit by applying local optimization tools which are moving rule, deletion rule and template matching. We apply moving rule or commutation rule [35] which is simply a matrix operation to see whether the adjacent gates commute or not. This operation is useful to reduce the gate count with the help of self inverse rule and template matching [36]. If at any point of time we find that the adjacent gates are of the same type and they form an identity (I) then we can remove both of the identical gates. This is called self inverse or deletion rule. In NCT gate library, all the gates are self inverse and in NCV gate library apart from the square root of Not gate (where $v.v^+ = I$) all the remaining gates are self inverse. In template matching [5] a sequence of gates is substituted by another sequence of gates having lesser number of gate count and same operational effect. Suppose we have a template: $U_1U_2U_3U_4U_5=I$ (where U_i is an unitary gate) and in the optimization procedure we come across a sequence of gates $U_2U_3U_4$ then we can replace this sequence of gates by $U_1^{-1}U_5^{-1}$.
3. In this step we obtain an equivalent primitive circuit. This is done by decomposing every n qubit gates (where $n \geq 3$) into equivalent circuit comprising of elementary gates (2×2 or 4×4 quantum gates).
4. We optimize the circuit comprising of quantum primitive gates in the following steps.
 - (a) We apply moving rule, deletion rule and modified template matching. In modified template matching

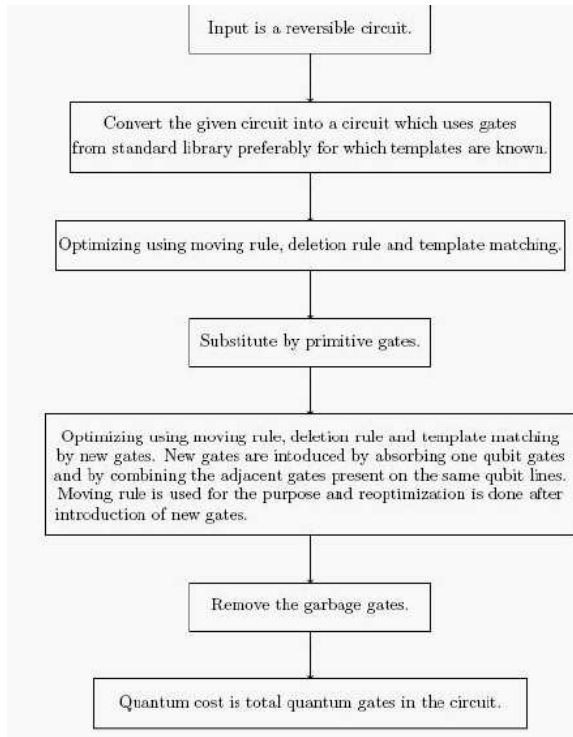


Figure 1 Algorithm for minimization of quantum cost.

a sequence of gates is substituted by another sequence of gates if it decreases the overall quantum cost of the circuit. In step 2 we have explained how a standard template matching reduces quantum cost by reducing the gate count. In modified template matching the overall cost is reduced by simultaneous application of template matching and introduction of new gates. Here we may substitute a sequence of gates by a larger sequence of gates if after the substitution, the gates present at the edge of the new sequence merges with the adjacent gates on the same qubit lines to reduce the overall quantum cost. It is explained in example 1 of this section.

- (b) We club together the adjacent gate/gates of dimension 2×2 and 4×4 , 4×4 and 2×2 , 2×2 and 2×2 , 4×4 and 4×4 to form new gates. In the circuit there may be other gates in the same qubit lines but not adjacent. In this step we will apply commutation rule and if the gates on the same qubit line or lines can be brought adjacent they will again form a new gate and reduce the cost. This is a modified optimization where we introduce new gate and apply the commutation rule to decrease the quantum cost of the circuit.
- (c) Since new gates are formed in the procedure, the existing gates in the circuit may belong to another gate library and it is possible that templates for

that particular gate library exist, hence we explore the further scope of minimization of gate count by template matching and deletion rule. We may require to generate new templates for this procedure.

5. We remove those gates, which do not affect the output or in other words affect only the garbage bits. When we substitute Toffoli gate by quantum primitives then there appear a lot of unnecessary quantum gates. This situation is similar to the garbage bits which are added to make an irreversible function reversible. Analogously these gates can be called as garbage gates. For example, if during computation the desired output of the circuit is obtained from the third qubit line in Fig. 2i then first two qubit lines at the output are garbage bits and the last two Cnot gates are garbage gates. Another example is a reversible function like $4 \bmod 5$ [32] (Grover's oracle) whose output is 1 if the 4 bit input is divisible by 5. The circuit has one desired output and rest of the output bits are garbage bits. In this case when we apply our quantum cost minimization algorithm we find it helpful to remove those gates (garbage gates) that affect only the garbage bits. This unique feature of quantum cost optimization algorithm is applied in the present work to minimize the cost of $4 \bmod 5$ d1 circuit⁴ (see Table I).
6. The quantum cost of entire circuit is obtained as the total number of quantum gates present in the circuit.

To illustrate how this algorithm works let us consider following two examples.

1) Consider a Fredkin gate and convert it to NCT circuit by applying a synthesis algorithm [5] as shown in Fig. 2a. We will calculate its quantum cost in two parts which is without optimizing the NCT circuit and after optimizing the NCT circuit. In the first part we substitute the Toffoli gate with its quantum primitives as shown in Fig. 2b. In Fig. 2c we have applied moving rule and indicated the movement by arrows. There are two places as shown in Fig. 2d where modified template matching can be applied and the resultant circuit is shown in Fig. 2e, here we have also marked the places where we can again apply templates. We obtain a circuit shown in Fig. 2f, we have marked in boxes the new gates and find that the quantum cost is 11. In the second part we will optimize the NCT circuit of Fredkin gate in Fig. 2a by applying template matching and obtain an optimized circuit as shown in Fig. 2g and further the Toffoli gate is substituted by primitives shown in Fig. 2h. We have applied modified optimization rule (commutation is shown by arrow) and in Fig. 2i we have shown the new gates formed. The quantum cost of the circuit is 5.

⁴ $4 \bmod 5$ d1 stands for the design number 1 given in benchmark to realize $4 \bmod 5$ function from NCT gate library.

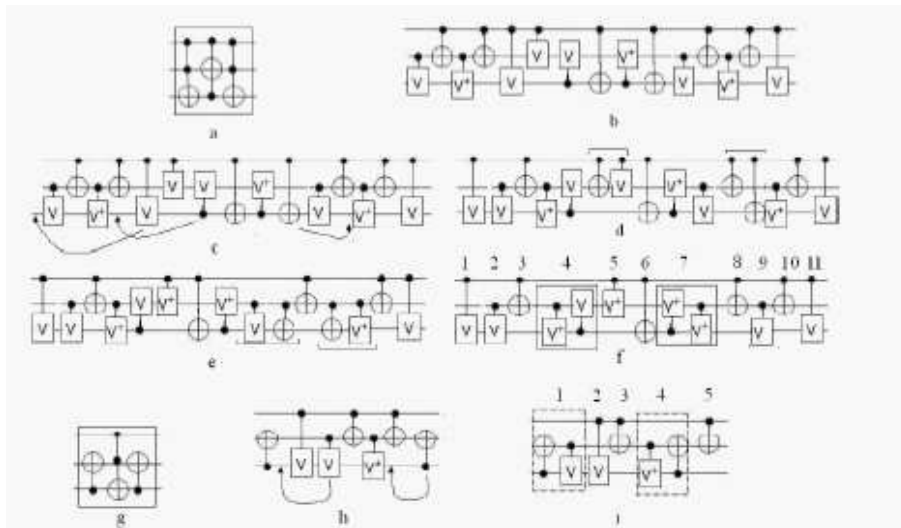


Figure 2 a) A Fredkin gate is implemented using three Toffoli gates. b) Toffoli gate is substituted by primitives, so its direct linear cost is $5 \times 3 = 15$. c) Moving rule is applied (the movements are shown by arrows), in d) and e) template matching rule is applied, f) and new gates are introduced (dashed boxes) and the quantum cost is 11. g) The circuit shown in Fig 2a is reduced here by template matching to one Toffoli and two Cnot gates. h) The Toffoli gate is substituted by quantum primitives. According to Mohammadi and Eshghi 's methods [4] the quantum cost is now 7. The moving rule is applied to circuit. i) New gates are introduced to yield quantum cost of Fredkin gate as 5.

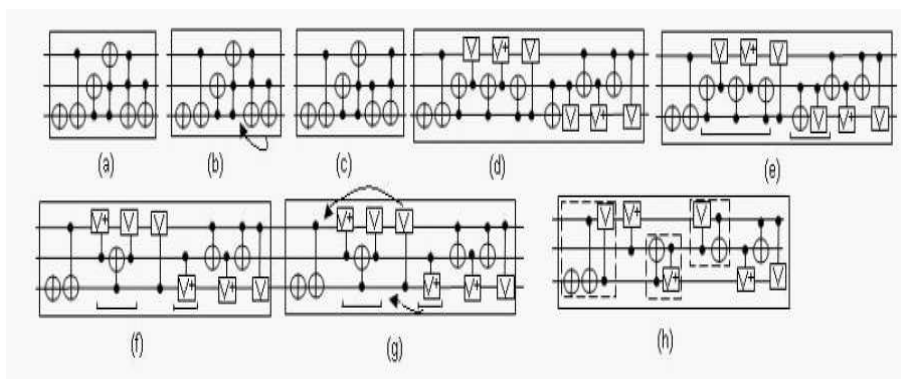


Figure 3 a) Reversible circuit for function 3.17 given in benchmark page of Maslov *et al.*[32]. b) Commutation rule is applied and arrow shows the movement of Cnot gate. c) NCT circuit before substitution of primitives. d) Quantum circuit of 3_17 function obtained by substituting the Toffoli gates with primitives. e) Template matching tool is applied from [36] to the circuit. f) Quantum circuit with reduced gate count. g) Modified local optimization rule is applied and two movements have been done in the circuit as indicated by the arrows. h) New gates are introduced (each dashed box is a new gate) and quantum cost of the circuit is obtained as the total quantum gates present in the circuit. The quantum cost of this circuit is 7.

This example clearly establishes that it is very essential to optimize the reversible circuit before substituting it with its quantum primitives. This aspect is not mentioned in earlier works [33,36,39,42]. It also clearly explains the meaning of modified template matching protocol introduced in the present work.

2) The reversible NCT circuit for function 3_17, is shown in Fig 3a [32]. This is the input of our algorithm, in Fig 3b we have shown that the end Cnot gate will commute with adjacent Toffoli gate (thereby reduce the quantum cost) and the movement is shown by an arrow. The resultant circuit after commutation is shown in Fig 3c. We try to optimize its gate count but we find that we cannot apply self inverse rule or template matching. We substitute the Toffoli gate with its primitives and the resultant circuit is shown in Fig. 3d. We try to optimize the circuit, there are two places shown in Fig 3e, where templates can be applied and after the application of templates, we have obtained the circuit which is shown in Fig 3f. Thereafter we apply modified optimization technique in Fig. 3g, new gates are formed which are shown in boxes in Fig 3h. Finally we calculate total number of quantum gates in the circuit and find the quantum cost of the circuit.

3.1. Quantum cost optimized circuits

We have already mentioned that most of the existing results related to quantum cost are available in benchmark page of Maslov *et al.* [32] and in Revlib [38]. In addition to these two databases Mohammadi and Eshghi [4], Gupta *et al.* [6] and Maslov *et al.*[36] have independently reported the quantum cost of different reversible circuits. We have compared the quantum costs reported in these works with the quantum costs of the same functions obtained using the present algorithm. The results of comparison are shown in Table I - Table III. To be precise in Table I we have compared the quantum costs of the following functions: i) mod5 function which is divisibility checker, ii) ham3 which is the size 3 hamming optimal coding function, iii) ham7 which is size 7 hamming optimal coding function, iv) hwb4 which is the hidden weighted bit function [47] with parameter $N=4$, v) 3_17 which is the worst case scenario 3 variable function [5] having function specification $\{7, 1, 4, 3, 0, 2, 6, 5\}$ and vi) 4_49 which is the worst case scenario 4 variable function [5] having function specification $\{15, 1, 12, 3, 5, 6, 8, 7, 0, 10, 13, 9, 2, 4, 14, 11\}$. Here we would like to note that in this paper we have mentioned the circuits described in [32] as benchmark circuits. To provide specific examples and to establish the superiority of our algorithm we have applied our algorithm to those benchmark circuits. Further, the benchmark circuits reported in [32] to realize a particular function is not unique and consequently different designs for the same purpose are marked with different indices, for example d1 denotes design 1, d2 denotes design 2 etc. Here we have followed the same convention as it is used in [32]. Gupta *et al.* [6] have synthesized few reversible circuits for realization of above mentioned functions in the form of a network of Toffoli gates and have also reported their quantum costs. Further in [36] improved quantum costs are reported for various circuits reported earlier [32]. We have compared the quantum costs reported in these works in Table I.

Circuit	QC	QC [32]	QC [36]	QC [6]	QC [38]
mod5 d1	24	24	14	-	9
mod5 d2	25	19	11	-	8
mod5 d3	13	13	9	13	8
mod5 d4	6	7	-	-	6
ham3 d1	6	7	7	9	5
ham3 d2	10	10	-	-	6
ham7	49	49	40	-	36
3_17	14	12	20	14	7
hwb4	23	23	23	-	16
4_49	40	32	29	-	28
4_49	32	32	27	-	21

Table 1: Comparison of quantum cost using our algorithm with the existing works of Maslov *et al.* [32], Maslov *et al.* [36] and Gupta *et al.*[6]

In Table II we have reported quantum cost of circuits from Revlib [38]. To be precise, we have compared quantum cost of the following functions: i) miller gate, ii) 3_17 which is the worst case scenario 3 variable function [5] and iii) different designs of decode 24 function which is 2 to 4 binary decoder. Table III compares quantum costs of some circuits that has been reported in [4]. For example: i) two bit binary adder with carry input using one constant input (see Fig. 3a of [4]), ii) two bit binary adder with carry input using two constant input (see Fig. 3b of [4]), iii) 9's complement circuit without constant inputs (see Fig. 4a of [4]) and iv) 2×2 bit multiplier (see Fig. 15 of [43]).

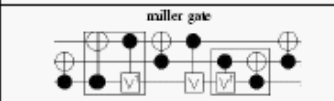
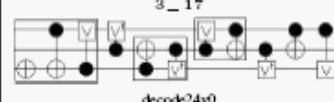
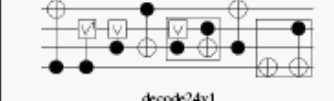

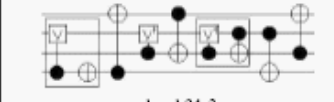
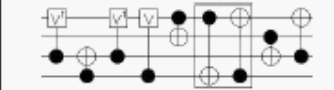
Circuit	QC	QC [38]	Ours
 miller gate	8	8	6
 3_17	10	10	7
 decode24v0	9	9	7
 decode24v1	9	9	7
 decode24v2	9	9	7
 decode24v3	9	9	8

Table 2: Comparison of quantum cost using our algorithm with the existing works of Revlib [38].

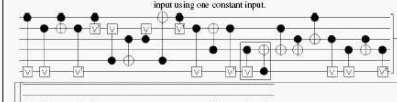



Circuit	QC	QC [H][43]	Ours
 Two bit binary adder with carry input using one constant input.	47	41	35
 Two bit binary adder with carry input using two constant input.	24	16	12
 9's complement	23	21	19
 2x2 bit multiplier	26	26	25

Table 3: Comparison of quantum cost using our algorithm with the existing works of Mohammadi [4,43].

The algorithm may be applied to other benchmark circuits too but to do so either one has to develop templates for the corresponding gate library or convert the circuit into other gate library for which templates has been provided in literature example NCT gate library. In Table IV, we have calculated quantum cost of some pure quantum circuits like EPR, quantum teleportation and shor code. Since quantum cost of these circuits have not been reported earlier, therefore its comparison could not be done. The quantum cost optimized circuits are shown in the first column of Table I - Table IV. The gates shown in the box

form a new gate and it would be counted as a single gate in the calculation of quantum cost.

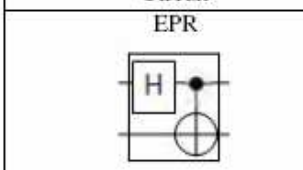
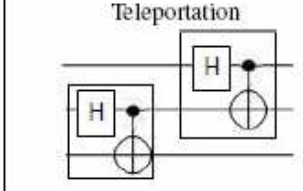
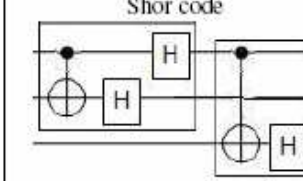
Circuit	QC	QC
 EPR	2	1
 Teleportation	4	2
 Shor code	5	2

Table 4: Quantum cost of important quantum circuits.

4. Conclusions

We have proposed an algorithm for minimization of quantum cost. We have applied our algorithm to different circuits from various sources [4,6,32,36,38,43] and compared our results. The outcome of the comparison (see Table I - Table III) clearly shows that the proposed algorithm produces best result. In Table IV we have reported quantum cost of different quantum circuits (for example, quantum teleportation, EPR circuit etc.). Through these examples it is clearly established that the proposed algorithm is useful in reduction of quantum cost. Thus the present algorithm provides a window for reduction of quantum cost of other circuits in future.

References

- [1] R. Landauer, Irreversibility and heat generation in the computing process, *IBM J. Res. Develop.* **5** (1961), 183–191.
- [2] P. Kerntopf, A new heuristic algorithm for reversible logic synthesis, in *Proceedings of the IEEE Design Automation Conference* (2004), 834–837.
- [3] A. Agrawal and N. K. Jha, Synthesis of reversible logic, in *Proceedings of IEEE, Design, Automation and Test* **2** (2004), 1384–1385.
- [4] M. Mohammadi and M. Eshghi, On figures of merit in reversible and quantum logic designs, *Quant. Infor. Pro.* **8** (2009), 297–318.
- [5] D. M. Miller, D. Maslov and G. W. Dueck, A transformation based algorithm for reversible logic synthesis, in *Proceedings of 40th Design Automation conference* (2003), 318–323.

- [6] P. Gupta, A. Agarwal and N. K. Jha, An algorithm for synthesis of reversible logic circuits, in *Proceedings on computer aided design of integrated circuits and systems* **25** (2006), 2317–2330.
- [7] A. Younes, Synthesis and optimization of reversible circuits for homogeneous boolean functions, *quant-ph/0664v1* (2007), 1–17.
- [8] H. Thapliyal and M. B. Srinivas, Novel reversible multiplier architecture using reversible TSG gate, *IEEE Int. Conf. Computer Systems and Applications* (2006), 100–103.
- [9] M. Shams, M. Haghparast and K. Navi, Novel reversible multiplier circuit in nanotechnology, *World Appl. Sci. J.* **3** (2008), 806–813.
- [10] M. Haghparast *et al.*, Design of a novel reversible multiplier circuit using HNG gate in nanotechnology, *World Appl. Sci. J.* **3** (2008), 974–978.
- [11] M. S. Islam *et al.*, Low cost quantum realization of reversible multiplier circuit, *Information technology journal*, **8** (2009), 208–213.
- [12] M. Haghparast *et al.*, Optimized reversible multiplier circuit, *JCSC* **18** (2009), 1–13.
- [13] A. Banerjee and A. Pathak, An analysis of reversible multiplier circuits, *International Conference on Emerging Trends in Engineering and Technology ICETET2010*, BITS, Goa, India, Nov. 2010, doi: 10.1109/ICETET.2010.70.
- [14] C. H. Bennett *et al.*, Teleporting an unknown quantum state via dual classical and EPR channels, *Phys. Rev. Lett.* **70** (1993), 1895–1899.
- [15] C. H. Bennet and G. Brassard, Quantum cryptography: public key distribution and coin tossing, in *Proceedings of the IEEE International Conference on Computers, Systems, and Signal Processing* (1984), 175–179.
- [16] C. Bennett and S. J. Wiesner. Communication via one- and two-particle operators on Einstein-Podolsky-Rosen states. *Phys. Rev. Lett.* **69** (1992), 2881–2884.
- [17] P. W. Shor, Scheme for reducing decoherence in quantum computer memory, *Phys. Rev. A* **52** (1995), R2493–R2496.
- [18] C. Branciard *et al.*, Security of two quantum cryptography protocols using the same four qubit states, *quant-ph/0505035* (2005), 1–19.
- [19] A. M. Steane, Error correcting codes in quantum theory, *Phys. Rev. Lett.* **77** (1996), 793–797.
- [20] A. R. Calderbank and Peter W. Shor, Good quantum error-correcting codes exist, *Phys. Rev. A* **54** (1996), 1098–1105.
- [21] P. W. Shor, Fault-tolerant quantum computation, in *37th Annual Symposium on Foundations of Computer Science* (1996), 56–65.
- [22] D. P. DiVincenzo and P. W. Shor, Fault-tolerant error correction with efficient quantum codes, *Phys. Rev. Lett.* **77** (1996), 3260–3263.
- [23] D. Gottesman, A theory of fault-tolerant quantum computation, *Phys. Rev. A* **57** (1998), 127–137.
- [24] L. Grover, Quantum computers can search arbitrarily large databases by a single query, *Phys. Rev. Lett.* **79** (1997), 4709–4712.
- [25] Quantum Circuit Implementing Grover’s Search Algorithm, <http://demonstrations.wolfram.com>.
- [26] K. A. Brickman, Implementation of Grover’s quantum search algorithm in a scalable system, *Phys. Rev. A* **72** (2005), 050306–050310.
- [27] M. Gupta *et al.*, Non-destructive orthonormal state discrimination, *quant-ph/0507096* (2005), 1–11.
- [28] Y. Takahashi, N. Kunihiro, A fast quantum circuit for addition with few qubits, *Quantum Information and Computation* **8** (2008), 636–649.
- [29] V. Shende, I. L. Markov, and S. S. Bullock, Synthesis of quantum logic circuits, *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **25** (2006), 1000–1010.
- [30] A. Abdollahi and M. Pedram, Analysis and synthesis of quantum circuits by using quantum decision diagrams, in *Proceedings of Design, Automation and Test* (2006), 1–6.
- [31] C. Ruican *et al.*, Automatic synthesis for quantum circuits using genetic algorithms, *LNCS* **4431** (2007), 174–183.
- [32] D. Maslov, G. W. Dueck and N. Scott, Reversible logic synthesis benchmark page, <http://webhome.cs.uvic.ca/dmaslov/>, (2009).
- [33] J. A. Smolin and D. P. DiVincenzo, Five two-bit quantum gates are sufficient to implement the quantum Fredkin gate, *Phys. Rev. A* **53** (1996), 2855–2856.
- [34] A. Barenco *et al.*, Elementary gates for quantum computation, *Phys. Rev. A* **52** (1995), 3457–3467.
- [35] M. Nielsen and I. Chuang, *Quantum Computation and Quantum Information*, Cambridge University Press, (2000).
- [36] D. Maslov *et al.*, Quantum circuit simplification and level compaction, in *Proceedings of Computer-Aided Design of Integrated Circuits and Systems* **27** (2008), 436–444.
- [37] D. Maslov *et al.*, Quantum circuit simplification using templates, in *Proceedings of Design, Automation and Test* (2005), 1208–1213.
- [38] W. Robert *et al.*, RevLib: An online resource for reversible functions and reversible circuits, <http://www.revlib.org/> (2009).
- [39] M. Perkowski *et al.*, A hierarchical approach to computer-aided design of quantum circuits, in *6th International Symposium on Representations and Methodology of Future Computing Technology* (2003), 201–209.
- [40] D. Maslov and G. W. Dueck, Improved quantum cost of n bit Toffoli gates, *Electronics Letters* **39** (2003), 1790–1791.
- [41] D. Maslov, Reversible logic synthesis, *Ph. D Thesis* (2003).
- [42] W. N. N. Hung *et al.*, Quantum logic synthesis by symbolic reachability analysis, *Design Automation Conference* (2004), 838–841.
- [43] M. Mohammadi and M. Eshghi, Heuristic methods to use don’t cares in automated design of reversible and quantum logic circuits, *Quantum Inform. Process. J.* **7** (2008), 175–192.
- [44] K. Iwama, Y. Kambayashi and S. Yamashita, Transformation rules for designing Cnot based quantum circuits, in *Proceedings of Design Automation Conference* (2002), 419–424.
- [45] D. Maslov, G. W. Dueck and D. M. Miller, Toffoli network synthesis with templates, *IEEE Transactions on CAD* **24** (2005), 807–817.
- [46] D. Maslov, G. W. Dueck and D. M. Miller, Fredkin/Toffoli Templates for Reversible Logic Synthesis, in *Proceedings of the IEEE/ACM international conference on Computer-aided design* (2003).
- [47] B. Bollig *et al.*, On the complexity of the hidden weighted bit function for various BDD models, *Theoretical Informatics and Applications* **33** (1998), 33–103.



Anindita Banerjee is pursuing postdoctoral research in the area of synthesis, optimization and testing of reversible/quantum circuits. Having completed her B.Sc in Electronics from Xavier's College, Ahmedabad, M.Sc. in

Electronics from Gujarat University and PhD from IIIT she is now at Bose Institute, Kolkata, India.



Anirban Pathak is Professor in the Department of Physics, IIIT. He has done his M.Sc and PhD from Department of Physics Visva Bharati. He has joined IIIT University in August 2002. During his PhD work and afterwards

he has published several papers in reputed journals. He was a category A speaker in the Theoretical Physics Seminar Circuit (TPSC). At present he has active research collaborations with different research groups in India, Argentina, Canada and Germany. His major research interests are: Quantum Optics, Circuit Theory, Mathematical Physics and Quantum Computing.