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Synthesis and Study of Annealing Effect on Electrical Properties of CdS doped Zn Thin Films

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Abstract: CdS doped Zn thin films have been prepared by thermal evaporation technique on glass substrate at room temperature under high vacuum of 10^{-5} mbar. These films have been annealed at different annealing temperatures (373,423,473 and 523) K. X-ray diffraction studies show that the structure is nearly crystalline with preferential orientation along the (111) direction of the cubic structure type. Results showed that the D.C. conductivity increases with increasing of temperature while it decreases with increasing of annealing temperatures. The activation energies increased with increasing of annealing temperatures. Hall measurements showed that all doped films are n-type. The charge carriers concentration decreases with increasing of annealing temperatures. Hall mobility, drift velocity, carrier life-time and mean free path increases with increasing of annealing temperatures.

Keywords: CdS:Zn, electrical properties, conductivity, thin film.

1. Introduction

Group II-VI compounds, in general, and CdS:Zn in particular have a high photosensitivity in the region of the electromagnetic spectrum [1]. The optical and electrical properties, as well as, its good chemical and mechanical stability recommend CdS:Zn as a semiconductor well suited for optoelectronic applications. They have an immense potential in photovoltaic applications [2-4] and as a luminescent materials [5-7]. Among these, CdS is an n-type direct band gap (2.4ev) semiconductor material and is widely used as a window layer for $CuInSe_2$, CdTe based solar cells [8]. Efficiencies of these solar cells are not too high due to the mismatching of lattice parameters and also of band gap.

By introducing Zn into CdS materials, CdS:Zn alloy semiconductors is formed and its band gap lies between 2.4 ev (CdS) and 3.6 ev (ZnS) at room temperature in the bulk sate. The band gap energy of the ternary alloy semiconductors could be tuned in the range of binary semiconductors band gap. CdS:Zn is an important material for solid state devices such as, solar cells, thin-film transistors, and light-emitting diodes. CdS:Zn often possesses P-type conductivity in bulk as well as in thin film form, which made it useful in many applications [9]. Hence for a better possibility of increasing the efficiency of a solar cell, tunable band gap material like $Zn_xCd_{1-x}S$ or $Zn_xCd_{1-x}Se$ are required.

There are several reports on the properties of CdS:Zn films prepared by various techniques such as molecular beam epitaxy (MBE) [10], chemical vapor deposition [11], spray pyrolisis [12], screen printing [13],

sol-get [14], simultaneous evaporation [15], true liquid crystalline templating [16], and solution grown technique [17]. In this paper, CdS:Zn thin films were prepared using evaporation technique. The structural and electrical properties of these compounds were investigated as a function of annealing temperature.

Experimental details

CdS doped Zn thin films were prepared by thermal evaporation technique onto glass substrates under vacuum 10^{-5}mbar. The CdS powder was doped with (1wt %) of Zn (99.99% purity). The thickness of films was 250nm. XRD patterns for CdS:Zn films carried out using a Phillips X–ray diffractometer system which records the intensity as a function of Bragg angle. The source of radiation was CuK_{α} with wavelength λ = 1.5405 Å, the current was 20 mA and the voltage was 30 kV. The scanning angle 2θ was varied in the range of (20–70) degree with speed of 2cm.min^{-1} . Optical transmittance was recorded with a double beam Shimadzu UV-VIS spectrophotometer in the wavelength range 300–1100 nm. The effect of annealing temperatures on the electrical properties was investigated.

Results and Discussion

1. Structure Properties

To demonstrate the effect of annealing, XRD pattern of the CdS doped Zn thin films deposited on glass at RT and annealed to 523 K is illustrated in Fig.(1 a and b) ,respectively. It is cleared from this figure that there is approximately one peak appeared at 2θ =26.591° for the RT film. This peak could be associated with the (002) reflection of the hexagonal modification or the (111) reflection of the cubic modification [18], While 2θ = 26.661° for the film annealed to 523K which is correspond to reflection from (111) plane of cubic phase. According to the American standard for testing materials (ASTM) card, these reflections represent a cubic structure having a zinc blend type. It is evident that the as-deposited film is of both hexagonal and cubic phase and the annealed film is converted hexagonal CdS films into the cubic phase but with a slight shift towards higher scattering angle. The shift towards higher scattering angle is the consequence of a decrease in the lattice parameter, probably due to a slight grain growth [17,19]. The cubic phase of CdS indicates smaller lattice parameter according to the diffraction angle (θ) compared to the hexagonal phase. This result agrees well with the reported data [20-22]. Comparison between observed and standard d-values for CdS:Zn and CdS thin films are listed in Table(1).

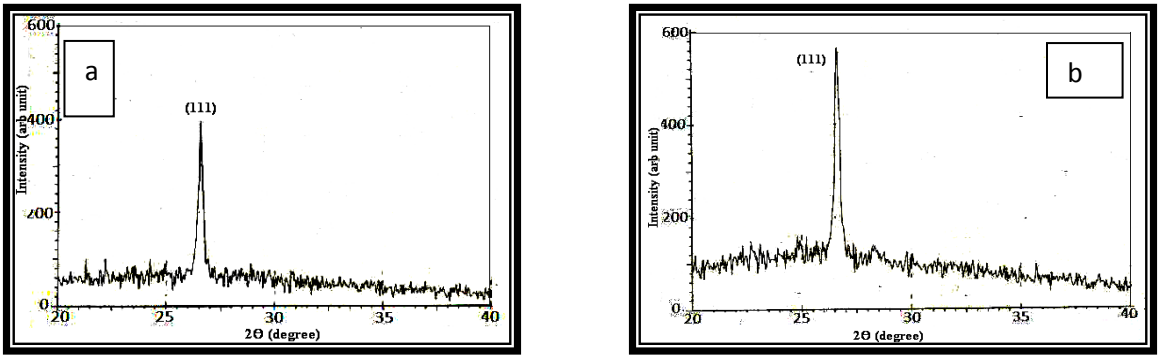


Figure 1: X-ray diffraction of Cds:Zn thin film at a: room temperature and b: 523K.

Table 1: gives the interplaner distance d, I/I_O, a, and D for R.T. and 523K samples in comparison with the standard values as in ASTM card.

Ta(K)	2θ (degree)	$d_{stand.}$ (Å)	$(I/I_O)_{stand.}$	d_{exp} (Å)	$(I/I_O)_{exp.}$	a(Å)	FWHM	(hkl)	D(Å)
RT	26.591	3.357	100	3.275	100	5.801	0.2678	111	5.302
523	26.661	3.357	100	3.240	100	5.787	0.2547	111	5.594

2. Electrical Properties

The variation of electrical conductivity as a function of temperature for different T_a of CdS doped Zn thin films is shown in Fig.(2). It is clear from this figure that the conductivity for all films increases with increasing of temperature and this agrees with the semiconductor behavior, while it is decreases with increasing of annealing temperatures from 373K to 523K. This arises from cumulative effect of grain size enhancement at grain boundaries (reduction of the number of grain boundaries due to the increase of the grain size) of the films**.** These results are consistent with other published results such as results of Haider et al. [23].

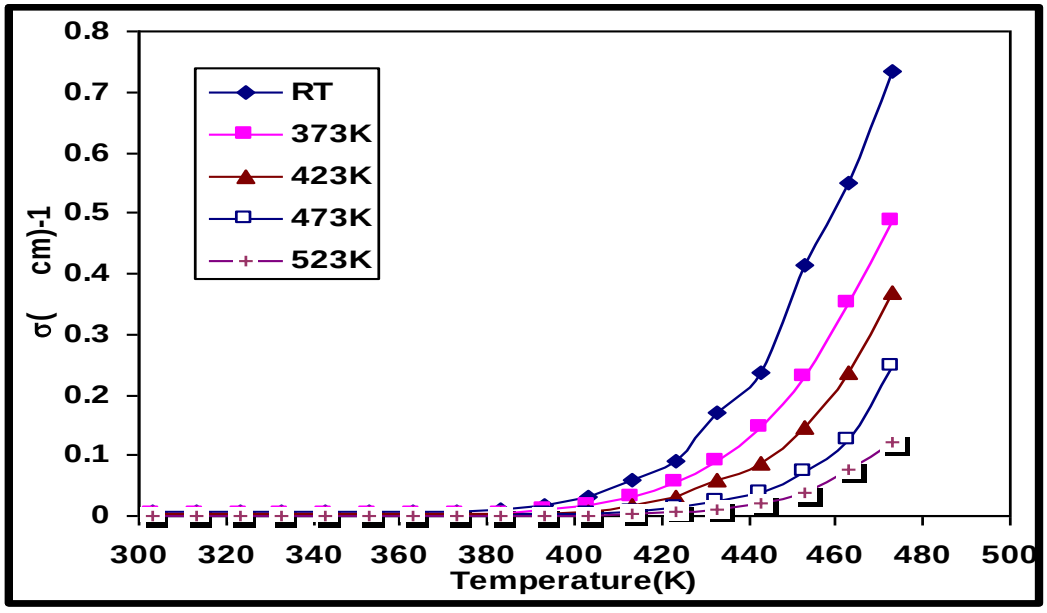


Figure 2: Variation of $\sigma_{D.C}$ versus temperatures for CdS:Zn films prepared at different annealing temperatures.

From Fig.(3) it can be observe that $\sigma_{R.T}$ decreases with the increasing of annealing temperatures, due to the rearrangement that may occur during annealing to higher temperatures.

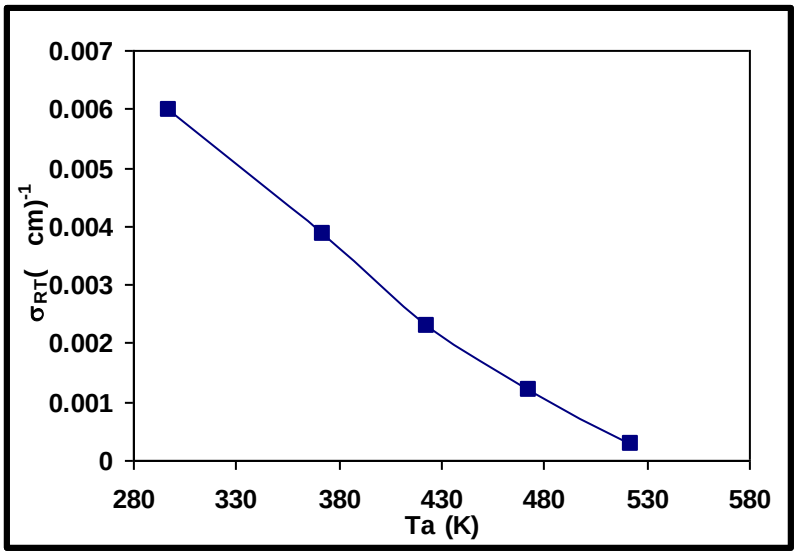


Figure 3: Variation of $\sigma_{R.T}$ versus Ta for CdS:Zn thin films.

In order to study conductivity mechanisms, it is convenient to plot logarithm of the conductivity (lnσ) as a function of 1000/T for CdS doped Zn thin films for different annealing temperatures, as shown in Fig. (4).

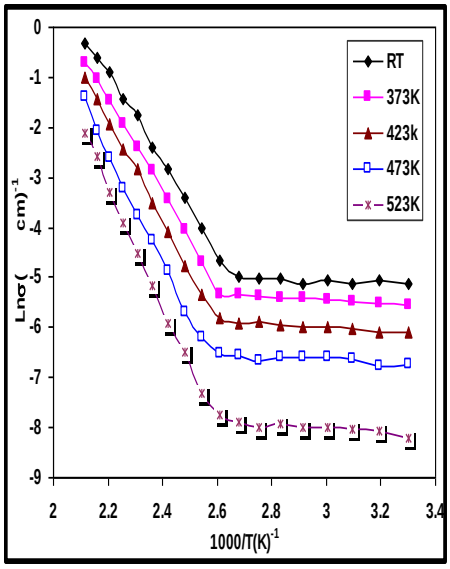
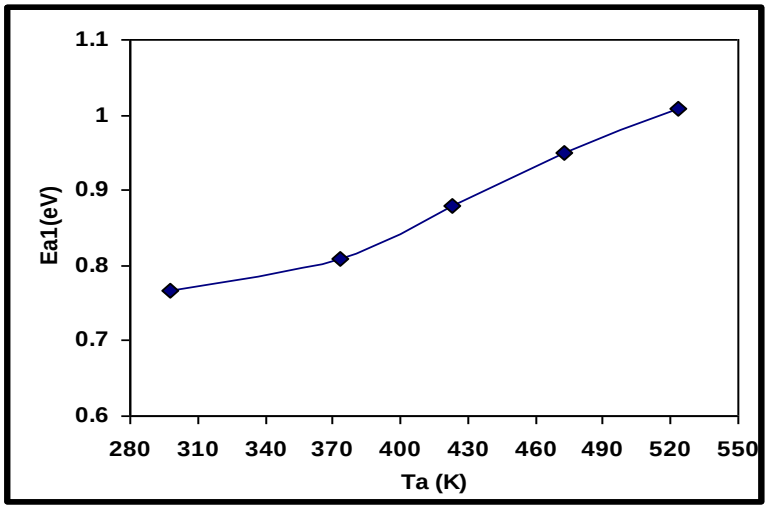
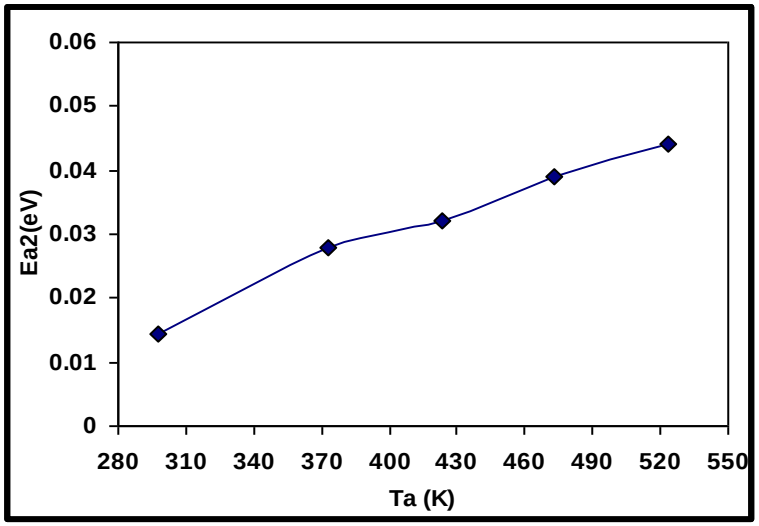


Figure 4: Lnσ versus 1000/T for CdS:Zn thin films at different annealing temperatures.

It is clear from this figure that there are two transport mechanisms, giving rise to two activation energies E_{a1} and E_{a2}. At lower temperature range (303 – 331) K, the conduction mechanism is due to carrier excited into localized states at the edge of the band whereas at higher temperature range (331–383) K, the conduction mechanism is due to carrier excited into the extended states beyond the mobility edge. Fig.(5 a,b) shows the effect of annealing temperature on both activation energies E_{a1} and E_{a2} for CdS:Zn thin films, respectively. It is obvious that the activation energies increase with increasing annealing temperatures.



a



b

Figure (5 a,b): Variation of Ea_1 and Ea_2 versus Ta for CdS:Zn thin films.

D.C. conductivity parameters for CdS:Zn films at different annealing temperatures are listed in table (2).

Table 2: D.C. conductivity parameters for CdS doped Zn films at different annealing temperatures.

T_a (K)	$\sigma_{R.T} \times 10^{-3}$ $(\Omega.cm)^{-1}$	Ea_1 (eV)	Temp.Range (K)	Ea_2 (eV)	Temp.Range (K)
300	5.98	0.767	(303-383)	0.0143	(393-473)
373	3.85	0.81	(303-383)	0.028	(393-473)
423	2.29	0.879	(303-393)	0.032	(403-473)
473	1.195	0.95	(303-373)	0.039	(383-473)
523	0.275	1.008	(303-363)	0.044	(373-473)

The type of charge carriers, concentration (n_H), Hall mobility (μ_H), drift velocity (V_d), life-time (τ) and mean free path (ℓ) of charge carriers have been calculated from Hall coefficient (R_H) data and D.C conductivity. The results are listed in Table (3). It's been found that all CdS:Zn thin films with different annealing temperatures exhibit a negative Hall coefficient (n-type). The n-type conductivity of vacuum-deposited CdS:Zn films is normally attributed to the existence of excess Cd in the condensed films [24]. The variation of carriers concentration and Hall mobility with annealing temperatures of CdS thin films at different annealing temperatures are shown in Figs.(5 and 6) respectively. The n_H and μ_H were calculated by using the following equations:

$$n_H = -1/qR_H \quad \text{for electrons} \tag{1}$$

or

$$P_H = +1/qR_H \quad \text{for holes} \tag{2}$$

Hall's mobility (μ_H) can be written in the form [21]

$$\mu_H = \sigma / n.q \tag{3}$$

$$\mu H = \sigma |R_H| \tag{4}$$

From the Hall mobility measurements, τ, V_d and ℓ of the carriers have been calculated by using the following equations:

$$\tau = (\mu.m^*)/e \tag{5}$$

Where m* is the effective mass, and τ is the life time of the carrier.

$$v_d = \mu . E_n \quad (6)$$

Where E_n is the applied electric field.

$$l = v_d . \tau \quad (7)$$

It's been observed that the carries concentration and Hall mobility decrease while Hall mobility increases with increasing annealing temperature due to improving the crystallite size, and the recrystallization occurring due to this treatment leads to a growth of the main crystallite size.

The results are listed in Table (3). It can be notice that all these parameters approximately increase with the increasing of annealing temperatures.

Table 3: carries concentration, Hall mobility, τ, Vd and ℓ for CdS doped Zn films at annealing temperatures

T_a (K)	$\sigma_{R.T} \times 10^{-5}$ $(\Omega.cm)^{-1}$	$R_H * 10^5$ c m^2/C	n_H (cm^{-3}) $\times 10^{12}$	μ_H $(cm^2/V.s)$	$v_d \times 10^2$ (cm/s)	$\tau(s) \times 10^{-10}$	$l \times 10^{-10}$(cm)
300	18.01	0.0437	1.431	0.783	0.0326	2.11	0.00069
373	3.183	32.768	1.907	104.3	0.846	4.96	0.041
423	2.980	38.422	1.567	114.5	0.916	30.77	0.281
473	2.701	125.361	0.4805	338.6	12.54	91.61	11.486
523	0.577	687.301	0.091	396.94	18.26	107.27	19.587

Conclusion

From the obtained results, we can conclude the following. The structural investigation of CdS:Zn thin films by using XRD analysis showed that all films are nearly crystalline with a cubic zinc blend structure and the preferred orientations are (111). Also, the films show a slight shift towards higher scattering angles with increasing of annealing temperature. Electrical measurement showed that D.C conductivity

for all films decreases with increasing of annealing temperatures. There are two transport mechanisms of the charge carriers in the range of (303-473)K.

In general, the activation energies increase with increasing of annealing temperatures. Hall measurements showed that all doped films are n-type.

The charge carriers concentration decreases with increasing the annealing temperatures. Hall mobility, drift velocity, carrier life-time and mean free path increases with increasing of annealing temperatures.

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