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Communication and Interoperation for Field Bus Systems based on ARM and FPGA

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Abstract: Communication and interoperation are critical to modern industry. A reconfigurable intelligent gateway based on ARM and FPGA is proposed on the basis of current situation and developing trend of protocol converting to achieve communication and interoperation among heterogeneous field bus systems and TCP/IP network. The functional block diagram, hardware architecture, software structure and protocol converting and communication model of the gateway are presented. The proposed gateway has a strong intelligent control ability, flexibility, reliability, fast conversion speed, consolidated device description and upper-level interface. It can also be updated online, and used as protocol converter or stand-alone intelligent controller, and has great theoretical significance and practical value in the field of heterogeneous networks communication and interoperation.

Keywords: communication, interoperation, protocol converting, reconfigurable gateway

1 Introduction

In order to reduce time-to-market, power consumption and product costs while improving product quality and efficiency, industrial companies face many challenges. One of these challenges is enhancing collaborative and integrated production automation, which requires close interoperability among various sub-systems. Interoperability can be defined as the ability of two systems or more to communicate, cooperate and exchange data and services, despite differences in languages, implementations and executive environments or abstract models [1]. The basis of interoperation is smooth and real-time communication.

In the areas of manufacturing, building automation, power and energy plants and logistics, the modern automation systems are wildly used which have very often a distributed nature. The control system is consist of a large number of control, measurement and field devices, in order to achieve the good control effect the communication and interoperation among all the devices is a critical factor. Today, a trend towards the usage of Ethernet-based approaches can be observed providing a common hardware communication standard in the aforementioned applications areas. However, a high variety of communication protocols (i.e., standardized and vendor specific) are usually in use since they are provided by the control and I/O devices, as well as measurement units applied in industrial control applications. Moreover, also legacy systems with field bus protocols have to be integrated in larger applications, such as FF, CAN, Profibus, Modbus, Lonworks, DNP3 [2,3].

The vision of only using one hardware and software standard covering all communication needs and requirements in industrial-process measurement, control, and automation systems is still a high-level goal and a nearly unreachable challenge in real-world applications so far [4]. For example, the field-buses varied from protocol, data format, structure, media, application field, etc.. So they cannot communicate to each other directly, not to mention the interoperability. In order to solve this problem, gateway and middleware are used to perform protocol converting among heterogeneous field bus networks.

1.1 Protocol Converting Gateway

In general, field bus protocol is based on ISO/OSI Open Systems Interconnection model. A typical field bus

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protocol contains physical layer, data link layer, the network layer, application layer and user layer. Each field bus has its own definition of the layers, so the protocol conversion is taken place mainly on data link layer, application layer and user layer by a MCU+ASIC architecture gateway [5], which is illustrated in Figure 1.

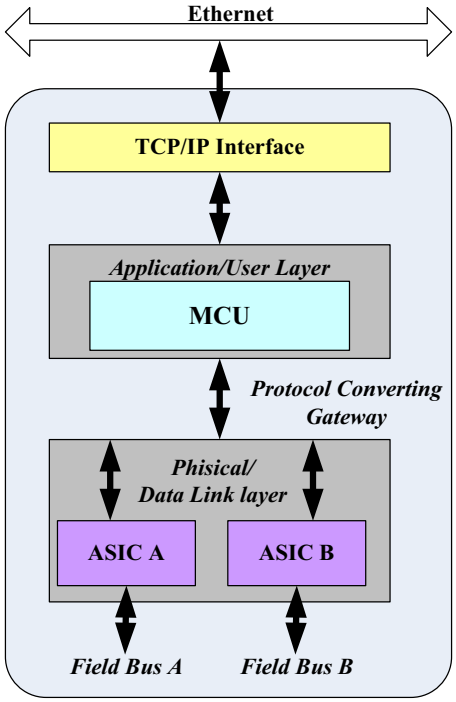

Fig. 1: Protocol Converting Gateway Based on MCU+ASIC.

The MCU+ASIC protocol converting gateway has simple structure and easy to be implemented. It can convert protocol among field bus A, field bus B and Ethernet. The ASIC contains the physical layer and data link layer, is the bottom-level data transceiver. The MCU is the application layer and user layer, complete the data mapping and format conversion [6]. This kind of gateway is widely used in the industrial automatic control. However, the following deficiencies are also exposed in practical applications.

- Poor expansibility and upgrade ability. If the protocol was changed during the field equipment upgrade, or a new sensor and actuator with different protocol was added into the network, the gateway would lose its functions.
- Limited processing capacity. In some kind of broadcast network, the irrelevant data should be filtered on the bottom layer, but the data was processed on the upper layer in existing gateway which impairs the system's processing power and real-time performance.
- Lack of control ability. In order to reduce the communication and ensure the real-time performance of large distributed system, data preprocessing and some simple control function should performed on the field, while the existing gateway is without this ability.

1.2 Interconnection Middleware

The middleware has standard communication interface and protocol, and is used in some heterogeneous network interconnection [7,8]. Regardless of the change and update of bottom layer system software, as long as the middleware was updated and the interface remained unchanged, the upper software can remain unchanged.

The existing heterogeneous network interconnection middleware is mainly based on OPC, DDE and ODBC, etc, Figure 2 is the middleware module based on OPC interface. However the middleware can not satisfy the real-time performance and data security requirements, and lacks bottom layer hardware support [9].

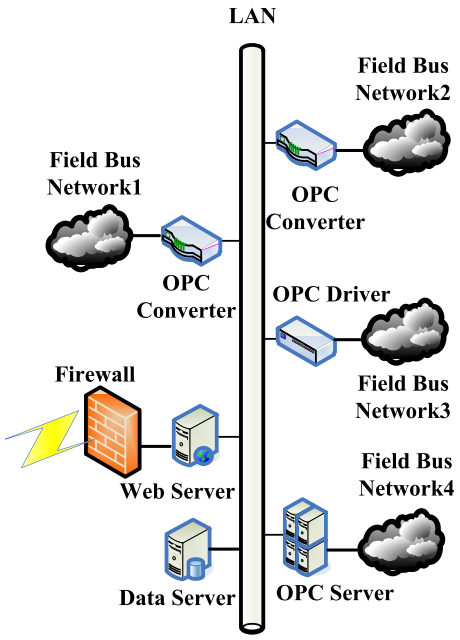

Fig. 2: Middleware Module Based on OPC Interface.

1.3 Aim of the research

Through the above analysis, we can see that the off-shelf gateway and middleware are insufficient in terms of intelligence, flexibility, online update, real-time performance, control ability, etc. with the constantly emerging of new control technology, sensors and actuators.

In this context, we have developed an innovative reconfigurable intelligent gateway based on ARM and FPGA to achieve heterogeneous networks communication and interoperability which combining the advantages of current protocol converting gateway and middleware, and has better intelligence, flexibility, scalability.

Therefore, the paper is organized as follows: Section 2 presents the architecture, protocol converting and communication model of the proposed reconfigurable

intelligent gateway. Section 3 describes an implementation of the gateway, several tests in detail, and research prospects. Finally, Section 4 will conclude the paper.

2 System Architecture

In order to achieve close interoperability among heterogeneous field bus networks, a reconfigurable intelligent protocol converting gateway is proposed according to the developing trends of heterogeneous network communication and interoperability [10,11], and the shortcomings of the existing gateway and middleware.

2.1 Hardware Architecture

The desired functions of the reconfigurable intelligent gateway is as follows.

– Protocol conversion among different field-bus and TCP/IP networks,
– Conversion at different levels,
– Online update,
– Data processing and control ability,
– Remote access and control,
– Unified device description and upper-level interface [12].

Powerful data processing unit, rapid online update, protocol conversion at different levels, remote access interface, unified description are needed for the gateway to fulfill the above functional requirements, and the corresponding designed hardware structure is illustrated in Figure 3.

Since ARM processors are using RISC based approach, they require significantly fewer transistors than processors that would typically be found in a traditional computer. The benefits of this approach are lower costs, less heat, and less power usage, that are desirable for industry automation, Internet equipment, set-top box, mobile communication etc., and are suitable for our gateway. FPGA has abundant programmable logic resources, and can be dynamically reconfigured for flexibility and augmentability.

The gateway contains multiple interfaces, large volume SDRAM and NVROM, convenient HMI, multi-I/O, A/D and D/A. Each network connects to FPGA through the specific interface chip. The FPGA is mapped to the memory space of ARM, and can be accessed either as I/O or memory.

2.2 Software Architecture

The system software is divided into two layers [13] as illustrated in Figure 4. The bottom layer is system software including Linux operating system and BSPs, the top layer is application software including the modules of control, data mapping, protocol package, WEB server, FPGA configuration, file transfer, power and clock management, login and security, SOAP, etc.

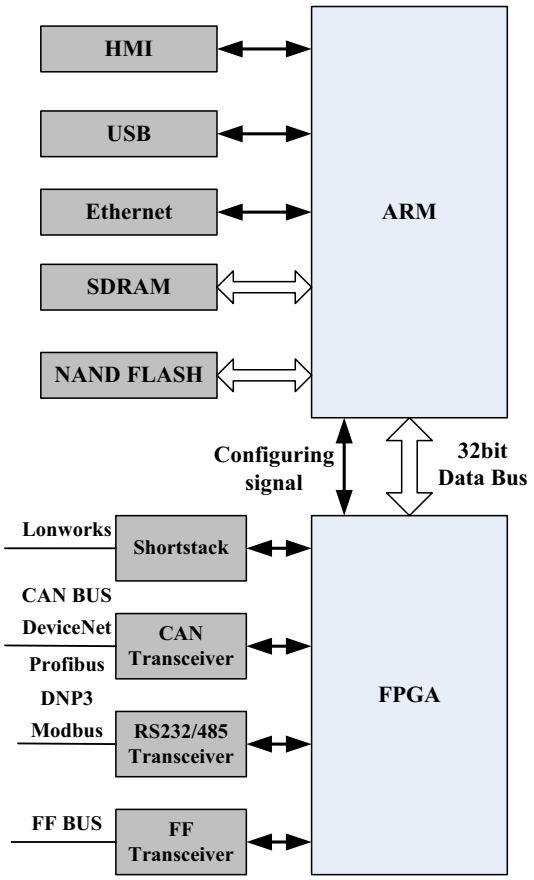

Fig. 3: Hardware Architecture.

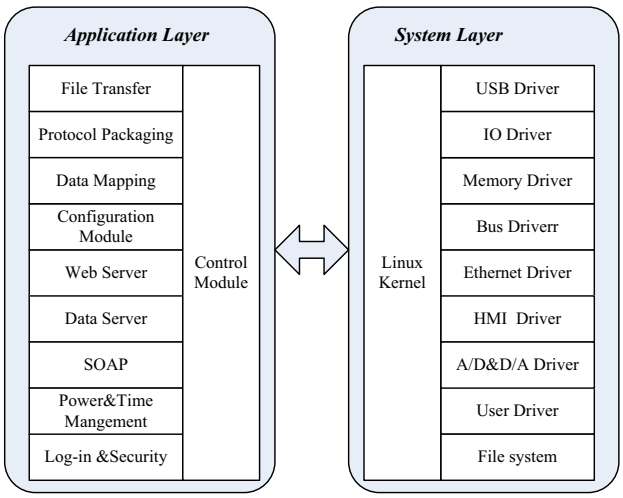

Fig. 4: Software Architecture.

2.3 Protocol Converting and Communication Model

The proposed protocol converting and communication model is illustrated in Figure 5 which contains multiple virtual nodes, communication management module, etc..

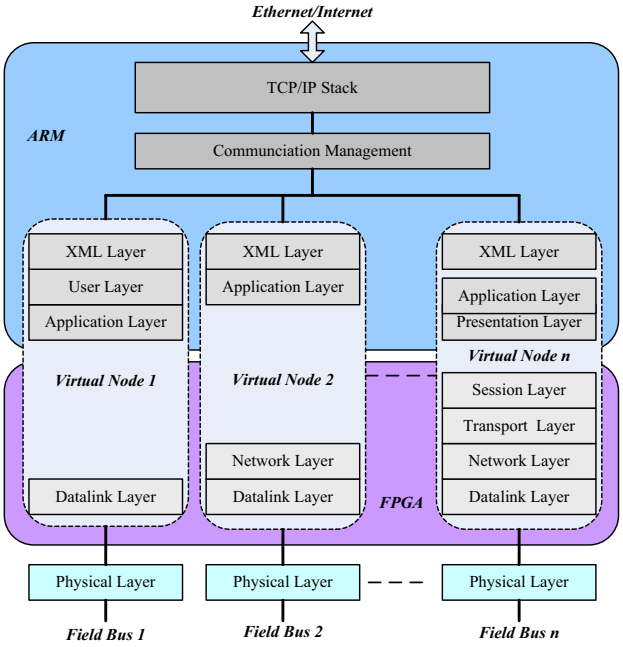

Fig. 5: Protocol Converting and Communication Model.

The converting algorithm, user specific functions and protocol stacks of each network are all packed into a virtual node. The virtual node acts and communicates in the same way as a real node, and there is no difference between the real and virtual nodes in the aspect of function. The gateway can contain multiple virtual nodes with different protocol at the same time.

The communication management module will establish a virtual channel when communication among virtual nodes and TCP/IP network occur and check the status of the whole link. If there is any fault in the link, messages will be sent to the upper-level. In order to ensure the real-time performance, several real-time event channels are reserved in the communication management module which have priority over ordinary channels [14].

The protocol parsing and converting are shared by FPGA and ARM, the FPGA is in charge of the data link layer, network layer and transport layer, ARM is responsible for the other upper layers. The deployment of FPGA makes the gateway possess the ability of rapid online update, if a new protocol is added or an existing protocol is modified, just reconfigure the FPGA [15]. ARM will establish and manage the virtual channel and real-time event channel, perform system resources managing, scheduling, data-mapping, and FPGA reconfiguration [16, 17].

In this way, the heterogeneous networks are integrated into one system. Data exchanging and interoperating are realized in real-time among different field buses and TCP/IP network with the ability of rapid online update, intelligent data processing, and being controlled through remote access interface and unified device description.

3 Implementation and Test

3.1 Implementation of the Gateway

There are three control systems in Zhangjiajie Railway Station, China. The BAS is based on CAN 2.0, public-address system and LED guidance system are using RS485 interface with HDLC protocol and self-defined application layer, the LED guidance system contains two kinds of data formats. These three systems were controlled by three computers separately, cannot communicate to each other. With the increase of passenger flow and demand of cost reduction, the three systems and TCP/IP network must be integrated together to achieve communication and interoperability.

According to the model presented above, we designed and implemented an embedded protocol converting gateway with SAMSUNG S3C2440 ARM9 processor, Xilinx XC3S200 FPGA, 256MB NAND FLASH, 128M SDRAM, two 100M Ethernet interface, one CAN bus interface, four RS485 interface, six inputs, six outputs, illustrated in Figure 6.

Fig. 6: Reconfigurable Intelligent Gateway.

The operating system is Linux 2.8.30, the kernel source code is tailored according to the requirement of the system. System resource scheduling, application layer and user layer and communication management are implemented within ARM processor, and the application software is just as Figure 4. XML description for the three systems, real-time status database and embedded WEB server are established for remote monitor and control, SOAP is used for the communication with upper-level software.

FPGA performs the parsing and packaging of data link layer, and includes five modules as shown in Figure 7. The structure of HDLC controller and CAN controller are shown in Figure 8 and Figure 9 [18, 19]. All these five modules are implemented with VHDL on the Xilinx ISE 9.1 developing environment, the resource consumption is shown in Table 1.

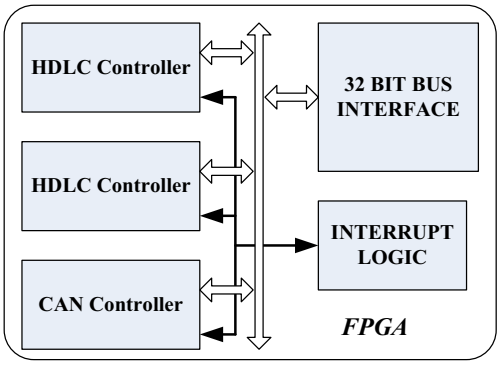

Fig. 7: Functional Diagram of FPGA.

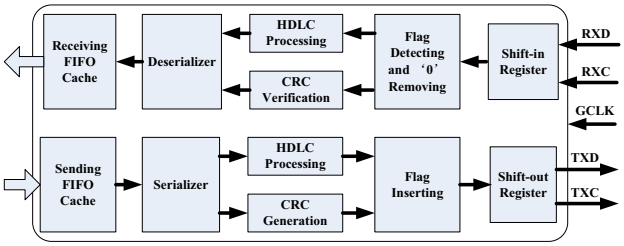

Fig. 8: Structure Diagram of HDLC Controller.

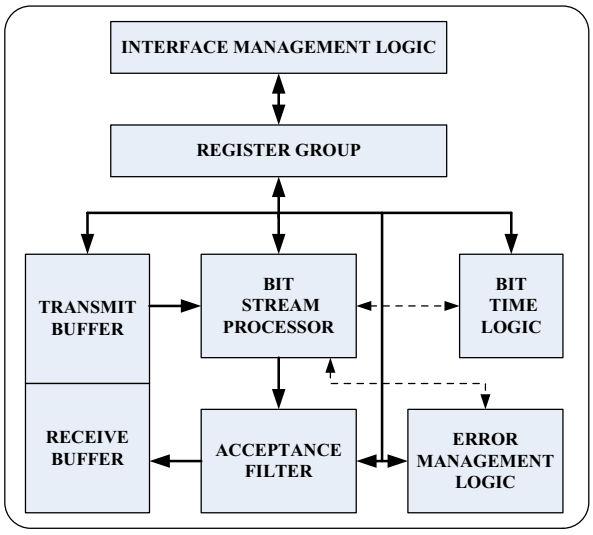

Fig. 9: Structure Diagram of CAN Controller.

Table 1: FPGA Resources Consumption

Logic Utilization	Used	Available	Utilization
Slice	1347	1920	70%
Flip Flops	1086	3840	28.3%
4 input LUTs	1712	3840	44.6%
BLOCK RAM	6	12	50%
GCLKs	4	12	33.3%

3.2 Test Results and Discussion

In order to verify the validity and reliability of the protocol converting, several loopback tests are performed between HDLC controller and CAN controller with two gateways, the test results are shown in Table 2, the baud rate is 115.2Kbps.

Table 2: Loopback Test Results

Direction	Number of Packet		
	Packets Sent	Packets Received	Packets Lost
CAN 2.0 → CAN 2.0	1003698	1003698	0
HDLC → HDLC	1003698	1003698	0
HDLC → CAN 2.0	1003698	1003698	0
HDLC → CAN 2.0 → HDLC	1003698	1003698	0

Continuous sending and receiving data packets, the internal registers have the same on two boards without an error. In other words, the gateway can achieve protocol converting and communication among heterogeneous networks, and the error rate of bit is less than 10-6, meeting communication requirements of the industry system.

The data transmission delay is tested based on ICMP protocol in two cases [20]. One case is HDLC Controller in FPGA, the other is HDLC Controller in ARM, and the test result is shown in Figure 10.

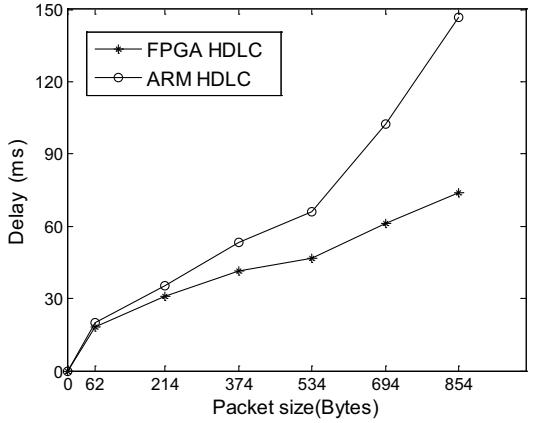

Fig. 10: Data Transmission Delay Test Result.

In the test, six different packet sizes were used which are 62, 214, 37, 534, 694 and 854 bytes. From Figure 10, we can see that:

– The delay of the former is smaller than the later.
– When the size of the packet increase, the delay is also increasing in both cases.
– The bigger of the packet size, the greater of the delay difference between the former and the later. For example, when the packet size is 62 bytes, the difference is 5%, but when the packet size is 854 bytes, the difference is nearly 100%.

We think there are two reasons for the above results:

– When HDLC controller is implemented in FPGA, the parsing and construction of HDLC protocol, the validation and generation of CRC code are processed in parallel. But when HDLC controller is implemented in ARM, all the tasks are processed in serial. Obviously, the former has a higher processing speed than the later.
– The later assigns parts of system memory, register and cache for HDLC controller, so there are less system resources for other tasks than the former and leads to performance degradation.

It can also be concluded from the test results that data link layer is critical to the system transmission delay. For the real-time system, it is the best choice to have the data link layer be implemented in hardware.

The dynamic reconfiguration of FPGA is also tested. The reconfiguration stream is stored in the external NAND FLASH, and the reconfiguration is controlled by ARM. There are two kinds of dynamic reconfiguration for FPGA, partial and whole reconfiguration. We use the whole dynamic reconfiguration and the reconfiguration time is about 10 seconds.

A fault-free operation of more than 5,000 hours shows that the gateway has provided fast communication channels among the three sub-systems and TCP/IP network, been seamlessly integrated with the upper-level software, simplified the system structure and improved the production efficiency.

3.3 Research Prospects

This paper has proposed a protocol converting gateway based on high performance ARM processor and reconfigurable FPGA for the communication and interoperability of industry automation. The gateway has great reliability, flexibility, scalability, can be used in the field of industrial automation, building energy-saving etc.. In order to make a more practical use, further study should be conducted with the following aspects:

– Test under heavy load, multi-node environment to find its limits,
– Test under mobile environment to satisfy the increasing need of mobile application,
– Explore new real-time communication algorithm to better meet the hard real-time application,
– Realization of partial dynamic FPGA reconfiguration, establish the IP library of common field bus protocol.

Interoperability is a high-impact productivity factor both within the private and the public sector, affecting the design of manufacturing operations, overall quality and yield time, as well as the cost of transactions [21]. Three levels of interoperability have to be considered [22]:

– the technical level,
– the organizational level,
– the semantic level.

Interoperability can therefore be achieved if and only if all three of these levels are fully completed [23]. This paper focuses on the technical part of the interoperability issue, which is to say, it deals with the field bus subsystems directly. However, we can achieve the organizational and semantic level interoperability by using the same strategy of combining hardware and software, focusing on flexibility and scalability and using standard interfaces.

4 Conclusion

In this paper, we have proposed an ARM+FPGA based protocol converting gateway for the communication and interoperability of industry automation which inherits the advantages of existing gateway and middleware, but with a better performance on intelligence, flexibility, Scalability and universality. We have also presented the functional block diagram, hardware structure, software structure and protocol converting model.

The gateway has rich logic control resources, multiple physical interfaces, strong intelligent data process and control ability, flexibility, reliability, consolidated device description and upper-level interface. It can also be updated online to accomplish communication and interoperation among various field buses and TCP/IP network. And when a new sensor or actuator is added to the network, just reconfigure the FPGA without having to replace the gateway, not only to improve the efficiency but also to protect the existing investment.

Simulated test results and the actual operation on a railway station have shown that the gateway has a fast converting speed, high reliability and flexibility. It can be used as a protocol converter or stand-alone intelligent controller and has a great theoretical significance and practical value.

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