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A New Hybrid Multilevel Inverter Topology for Medium and High Voltage Applications

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Abstract: In this article, a new hybrid multilevel inverter topology is proposed for medium and high voltage applications with new carrier based modulation techniques are presented. The performance of the developed topology has been realized in terms of a number of switches, gate driver circuits, and maximum blocking voltage. The proposed modulation technique produces a low Total Harmonic Distortion with improved fundamental component of Root Mean Square output voltage. Finally, 13-level laboratory based hardware test has been conducted and it has good agreement with simulation results.

Keywords: Multilevel Inverter, Carrier Based Modulation, Reduced Switches, Total Harmonic Distortion (THD), Maximum Blocking Voltage.

1 Introduction

The multilevel inverter is more popular than a conventional two-level inverter, because the medium voltage rating power semiconductor devices may be employed for high power application along with higher power quality. The multilevel inverters have offered a reduction of dv/dt stress, THD, and Electro-Magnetic Interference (EMI) over conventional two-level inverters. The traditional multilevel inverters are of following types: (i) Neutral Point Clamp (NPC), (ii) Flying Capacitor (FC), and (iii) Cascade H-Bridge (CHB). These topologies are successfully installed in real-time applications, like voltage or current compensation (FACTS devices), industrial drives, and bi-directional power flow in HVDC.

Among these multilevel inverters, the CHB has received a special attention due to its modularity and efficacy. The NPC converter is most widely used in all AC high-power applications in the range of 2.3 kV to 6 kV [1], and it is preferable for back-to-back power flow application. Because the single DC source is split by several DC-link capacitors [2] and it require a large number of clamping diode for unidirectional current flow. The voltage stress across the power diode increases as much as the level increases and the redundant state is less. The flying capacitor (FC) offers more redundant state with a number of the clamping DC-link capacitor. The electrolytic capacitors have more failure rate, and its reliability is low [3].

The detailed study about life prediction of electrolytic capacitors is discussed in [3]. In this, the life of various power components comparison is presented and its confirming that electrolytic capacitors have more failure rate, low reliability compared to other passive components. The CHB converter is a predominant multilevel converter because, it does not require any additional clamping diode or capacitor, so that, the reliability and modularity are good, but it requires an isolated dc sources.

However, in traditional topologies, the number of output level increases with the corresponding increase in power switches, which include an increase in the installation space, gate driver circuits, and total cost of the converter. A new cascaded multicell multilevel converter topology [4], which may operate in both symmetric and asymmetric modes with reduced on-state switches than conventional CHB. In the symmetric configuration, the magnitude of all the dc sources should be equal and the asymmetric configuration magnitude of dc source not

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equal, and this can be determined by different algorithms presented in [5]. The asymmetric configuration generates a large amount of output voltage level with fewer power switches with a different voltage rating of switches. However, the asymmetric topologies required variety of dc source voltage and balancing of each dc source is difficult.

The cascaded structure of new topologies is presented in [6, 7], in which the converters are optimized for different goals such as a number of dc sources, power switch, gate driver circuits, and blocking voltage. However, the number of switches and blocking voltages are high. For high-voltage applications, a new hybrid topology is proposed in [8] with reduced switch count. In the aforementioned studies, the number of maximum blocking voltage switches is four.

The main focus of the paper is, to improve the power quality and reduce the power switch count along with maximum blocking voltage in symmetric configuration is discussed. The input dc source can be provided through a multi-winding transformer or photovoltaic panel with dc/dc converter. This paper focused on the new hybrid multilevel inverter with novel carrier based modulation technique to minimize the output voltage harmonic profile.

The organization of this paper is development of proposed symmetric topology in Section 2. To reduce the blocking voltage on switches hybrid topology is presented in Section 3. In Sections 4 and 5 discussed the various comparison results and development of *u-n* shape carrier modulation technique. Finally simulation and experimental results with detailed values are presented in Section 6. The summary of the proposed topology and modulations with advantage and future works are presented in Section 7.

2 Development of Proposed Topology

The proposed generalized structure of new symmetric multilevel inverter topology is as shown in Fig. 1, which produces a staircase output voltage waveform near to sinusoidal curve. This topology requires less number of switches, gate driver circuits, and less installation space, comparable with CHB in symmetric configuration and other recent topologies [9–11].

The topology is constructed with a combination of single source unit (SS unit) and double source unit (DS unit). SS unit consists of single dc source with two power switches and DS unit comprises two dc source and two power switches as shown in Fig. 1.

The SS unit and DS unit together produced a stepped dc/dc output voltage waveform. The full bridge converter is connected with the load to convert stepped DC to stepped AC output voltage. The switching pattern for proposed topology is listed in Table 1 The proposed topology generates m level (N_{Level}) of output voltage for n number of dc sources with respect to switching sequence

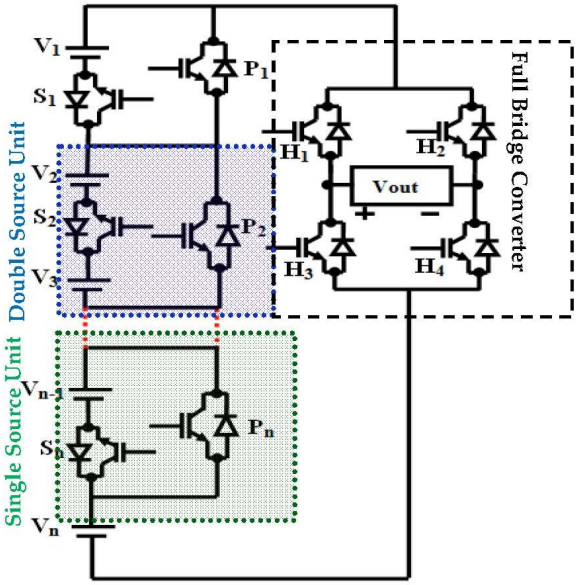


Fig. 1: Generalized structure of proposed symmetric topology.

as listed in Table 1, and the number of switches (N_{Switch}), gate driver circuits (N_{Driver}), and total blocking voltage (T_{Block}) of proposed topology are expressed in terms of n as follows:

$$\text{Number of levels: } N_{\text{Level}} = m = 2n+1 \tag{1}$$

$$\text{Number of Switches: } N_{\text{Switch}} = \begin{cases} n+5, & n = \text{odd} \\ n+4, & n = \text{even} \end{cases} \tag{2}$$

$$\text{Gate driver circuits: } N_{\text{Driver}} = \begin{cases} n+5, & n = \text{odd} \\ n+4, & n = \text{even} \end{cases} \tag{3}$$

Maximum Blocking Voltage of the full bridge unit $= nV_{\text{dc}}$.

The total maximum blocking voltage of all the switches is:

$$\text{T}_{\text{Block}} = 2 \times (\text{N}_{\text{Level}} + 2) \times \text{V}_{\text{dc}}. \tag{4}$$

However, this topology is not suitable for high-voltage applications because, the maximum blocking by full bridge switches is high.

3 Development of New Hybrid Topologies

The maximum blocking voltage in the full bridge inverter switches of proposed symmetric topology can be resolved by the development of new hybrid topology. The hybrid topology is a mixture or combined two different topologies, here, proposed symmetric topology and

Table 1: Generalized switching pattern for proposed topology.

State	Series/Parallel switches for dc/dc stepped output voltage										Voltage levels ($V_{0,\max}$)
	P_1	P_2	$P_3 \cdots$	P_{n-k}	P_n	S_1	$S_2 \cdots$	$S_{n-k} \cdots$	S_{n-1}	S_n	
1	1	1	1 $\cdots$	1	1	0	0 $\cdots$	0 $\cdots$	0	0	V_n
2	0	1	1 $\cdots$	1	1	1	0 $\cdots$	0 $\cdots$	1	0	V_0+V_1
3	1	0	0 $\cdots$	1	0	0	1 $\cdots$	0 $\cdots$	0	1	$V_0+V_{0-1}+V_1$
4	1	1	0 $\cdots$	0	0	0	0 $\cdots$	1 $\cdots$	1	1	$V_1+V_0+V_2+V_3$
$n-k$	1	0	0 $\cdots$	0	0	1	1 $\cdots$	1 $\cdots$	1	1	$\sum_{i=1}^{n-k} V_{n-k}$
$n-1$	1	0	0 $\cdots$	0	0	0	1 $\cdots$	1 $\cdots$	1	1	$\sum_{i=1}^{n-1} V_{n-1}$
n	0	0	0 $\cdots$	0	0	1	1 $\cdots$	1 $\cdots$	1	1	$\sum_{i=1}^{n} V_n$

existing packed H-bridge cell topology is used to form the new hybrid topology as shown in Fig. 2 This hybrid topology is consists of two part (i) recommended symmetric unit and (ii) basic unit. The basic unit developed with six switches ($S_1', S_2', S_3', P_1', P_2'$, and P_3') and two numbers of isolated dc sources. Since the hybrid topology is a symmetric method which uses the equal magnitude of dc source

$$V_1 = V_2 = V_3 = \cdots = V_n = V_1' = V_2' = V_{\mathrm{dc}}. \qquad (5)$$

The required number of switches, gate driver circuits and total blocking voltage for n number of dc source for the new hybrid topology is listed in the Table 2. The blocking voltage of individual switches can be determined as follows:

Table 2: Comparison of power component requirements for proposed hybrid topology.

Description	CHB	Proposed
Number of level	$2n+1$	$2nU+5$
Number of switches	$4n$	$\begin{cases} nU+6, & nU = \text{odd} \\ nU+8, & nU = \text{even} \end{cases}$
Number of Gate Driver	$4n$	$\begin{cases} nU+6, & nU = \text{odd} \\ nU+8, & nU = \text{even} \end{cases}$
Maximum Blocking Voltage	V_{dc}	$(N_{\mathrm{Level}}-3)\times V_{\mathrm{dc}}$
Total Blocking Voltage	$n\times V_{\mathrm{dc}}$	$6\times(nU+1))\times V_{\mathrm{dc}}$

(i) Upper Leg (Recommended symmetric topology):
- Maximum blocking voltage by switches in level generator part is V_{dc} and $2V_{\mathrm{dc}}$.
- Full bridge unit switches have maximum blocking voltage of nUV_{dc}.

(ii) Lower Leg (Basic Unit):
- Maximum blocking voltage by switches is V_{dc} and $2V_{\mathrm{dc}}$
- The sum of the blocking voltage of individual switches is called as total blocking voltage which determines the cost of the inverter.

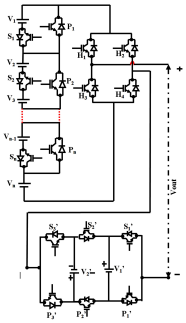


Fig. 2: Generalized structure of hybrid symmetric topology with basic unit of proposed topology.

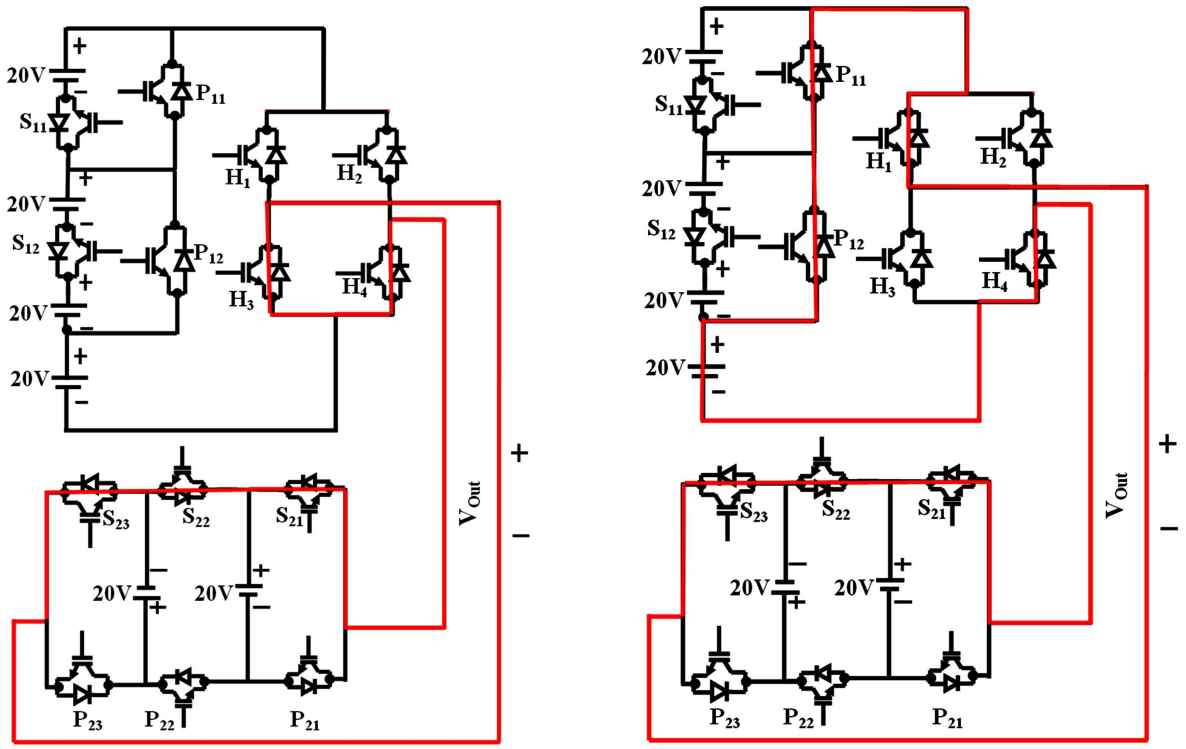
The number of switch depends on the source connected to the upper leg. The even number of DC source required less number of switches as compared to an odd number of DC sources. The components requirement for proposed hybrid topology and conventional CHB is presented in Table 2. The different operating mode of 13-level hybrid topology is depicted in Fig. 3. The Fig. 3 highlighted the positive half cycle modes and the negative half cycle mode is not depicted, and to obtain negative cycle waveform the switches H_2 & H_3 and P_1', S_2' and $'S_3$ has to be turned on.

Mode 1–4:

In this mode, V_1, V_2, V_3 and V_4 dc sources are delivering the current to the load. The switches S_1, S_2, P_1, and P_2 are alternatively turned on and off to produce the corresponding output voltage, at same time the switches P_1'–P_3' are also turned on to give the current path.

Mode 5–6:

The lower leg switches S_1'–S_3' and P_1'–P_3' are also alternatively turned on and off to produce the stepped



(a) 0 V **(b)** +20 V

Fig. 3: Different modes of operation of proposed multilevel inverter.

output voltage at the load Mode 0 In this mode, no voltage at the load but to provide the continuous current path through the switches H_1–H_2 or H_3–H_4 will be turned on. The one of the main advantage of proposed hybrid topology provides more redundant state which will increase the reliability of the system. For 13-level inverter, each level has the more than three redundant states except the $\pm 5V_{dc}$ and $\pm 6V_{dc}$. The modularity of hybrid topology is increasing by providing more optional switching sequences.

Total blocking voltage of hybrid topology is higher than the CHB but lower than the other topology as shown in Fig. 5 but here worth to mention that hybrid topology requires less number of switch compare to CHB which further reduces the layout size, gate driver circuits and minimize the switching pattern complexity. It is clear evident that proposed topology uses a minimum number of switches and reduced blocking voltage which again confirming that reliability of proposed topology is better than the other topologies.

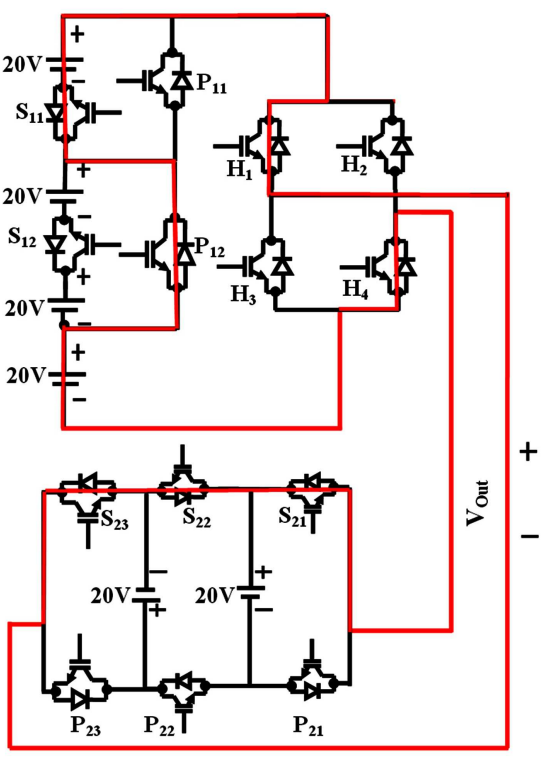
4 Comparison of Proposed Topologies with Conventional Cascaded H-bridge

To determine the proposed best topology for symmetric configuration, the following parameters are taken into account: N_{Level}, N_{IGBTs}, and T_{Block}. Fig. 4 shows the variation of N_{IGBTs} required to obtain N_{Level} output voltage. The proposed topology uses a minimum number of switches as compared to other topologies presented in the literature. The new hybrid topology offers more reliable, because it requires less number of power switches and gate driver circuits. For 13-level output voltage, CHB uses 24 IGBTs but a new hybrid topology requires 14 IGBTs, this will reduce the power losses.

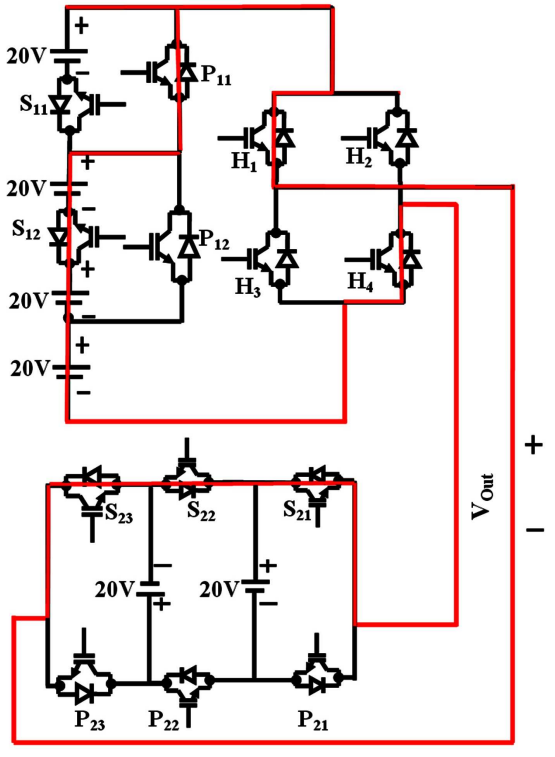
5 Proposed “u-n” Shape Carrier Modulation Technique

The Multicarrier PWM (MCPWM) techniques are most common pulse generating techniques in the multilevel inverter and this technique is classified into phase disposition, alternate opposition disposition and alternate phase opposition disposition [12, 13]. The advantage of MCPWM is producing low THD in output voltage at the load but the switching losses are high. The development of proposed carrier signal is shown in Fig. 6.

This carrier signal is extracted from the sinusoidal signal with higher frequency. The IGBT switches are chosen from the built-in library. The gating signals are



(c) +40 V



(d) +60 V

Fig. 3: continued..

generated using the modified carrier SPWM scheme is called "u-n Shape" PWM (u-n MCPWM) technique. However, the MCPWM Techniques THD is low at high switching frequency which will increase the switching loss and reduce the life of the devices. But in u-n MCPWM techniques produce low THD at the low switching frequency and improve RMS Voltage. The modulating signal is assumed to be a sinusoidal wave of unit amplitude and 50 Hz fundamental frequency. The switching frequency of the inverter is chosen as 1 kHz (this can be changed by varying the frequency of the carrier wave) and hence the frequency of the modified carrier wave is 1 kHz.

The gating pulse generation pattern is described as follows, the proposed carrier signal pattern is generated by means of multiplying high-frequency carrier sine signal with positive clipping function. Then, the multiplier output signal is inverted and processed through positive clamper and which is added with high-frequency negative clamped square wave signal for producing the positive portion of proposed carrier signal. Similarly, to obtain the negative portion by means of multiplying high-frequency carrier sine signal with negative clipping function. Then, the multiplier output signal is inverted and processed through negative clamper and which is added with high-frequency negative clamped square wave signal. The gating pulses are generated by realizing these two signals compared with modulating sine waveform as shown in Fig. 7.

Practically, the gate drive signals are complementary to prevent the two power switches of the same leg conducting simultaneously.

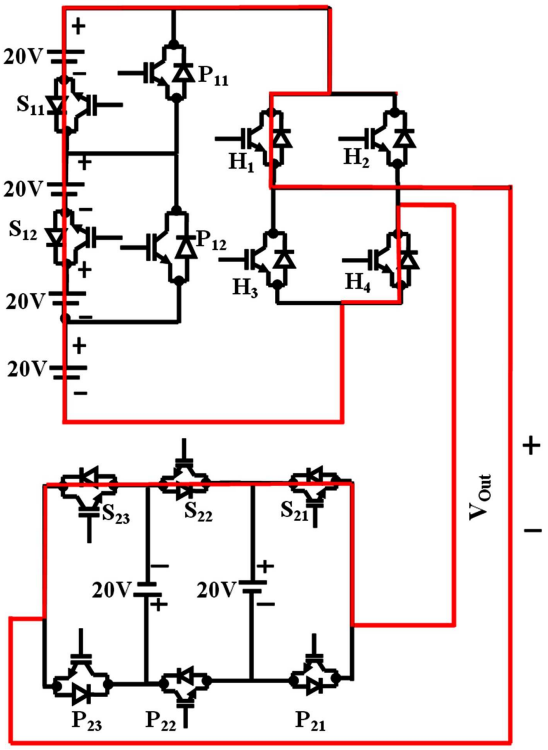
The generation of "u"shape carrier signal is extract from

Reference sinusoidal waveform is

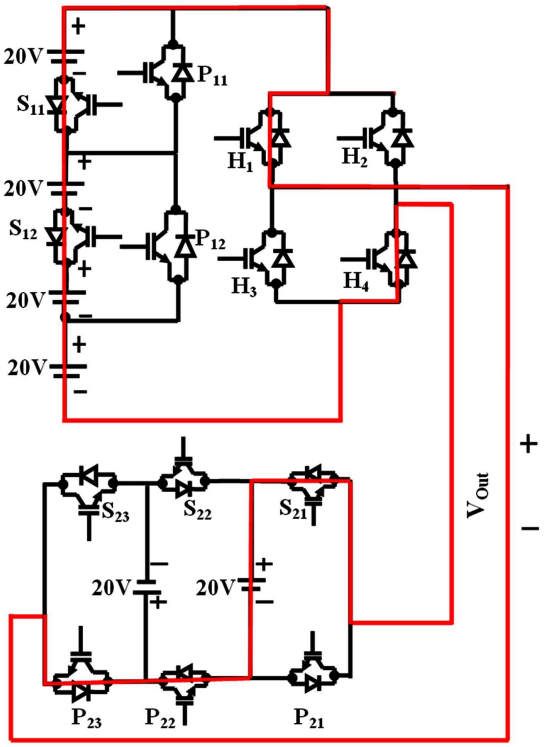
$$x(t) = V_m \times \sin(\omega t), \tag{6}$$

where V_m is the peak voltage.
For positive carrier signal generation ("u" Shape):
The generation of "u"shape carrier signal is extract from the carrier sinusoidal waveform and different level shifted can be achieved by selecting proper n value based on the level of inverter.

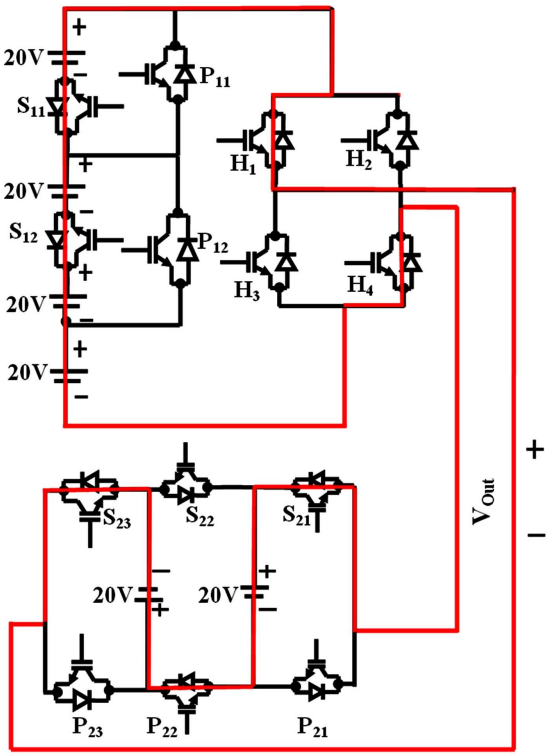
$$(V_c \sin(\omega t)) \times V_c \times \left[\frac{1}{2 \times f_{sw}}\right] \times (-1) + \text{bias}(+n). \tag{7}$$



(e) +80 V



(f) +100 V



(g) +120 V

Fig. 3: continued..

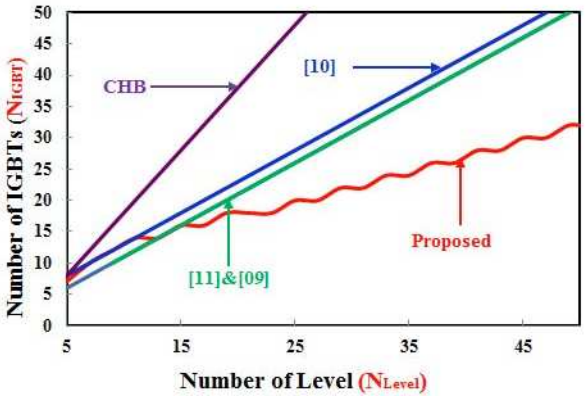


Fig. 4: N_{Level} vs. N_{IGBTs}.

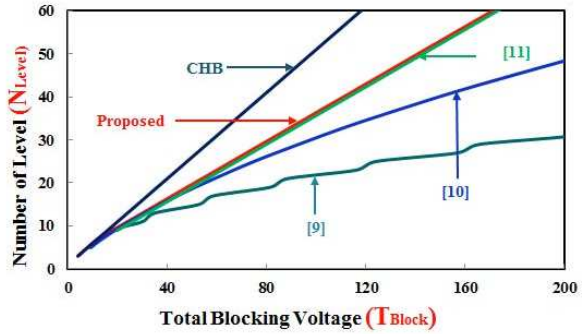


Fig. 5: N_{Level} vs. T_{Block}.

$(V_c \sin(\omega t))$ is reference of carrier signal.
For negative carrier signal generation ("n" Shape):

$$(V_c \sin(\omega t)) \times V_c \times \left[\frac{1}{2 \times f_{sw}}\right] \times (-1) + \text{bias}(-n) \quad (8)$$

where f_{sw} is the switching frequency.

$$V_O(t) = \pm[V_m \sin(\omega t)(\geq \text{ or } \leq) n \sin f_{sw}(t)] \quad (9)$$

where V_c is the carrier amplitude.
The comparison of reference and proposed carrier signal yields the desired pulse sequence for multilevel inverters.

From equation (9) the carrier signal amplitude with

$$D_1 = V_c \times \frac{1}{f_{sw}} \times 0.5 \times (-1) + \text{bias}(+n). \quad (10)$$

for 180° positive cycle with respect to duty cycle.

$$D_2 = V_c \times \frac{1}{f_{sw}} \times 0.5 \times (-1) + \text{bias}(-n) \quad (11)$$

for 180° negative cycle with respect to duty cycle.

Output Voltage Harmonic and RMS voltage is a major design issue in multilevel inverter topology and its modulation techniques. In order to improve the voltage harmonic profile, various modulation techniques are proposed. However, in this paper proposed a new modulation technique which reduces the harmonic distortion as compared to other carrier based modulation techniques and also the Output RMS voltage is increased.

To prove the high performance of proposed modulation technique is compared with other techniques for a 13-level inverter which is shown in Fig. 8 and 9. In Fig. 8 and 9 shows the total harmonics distortion and RMS output voltage respectively.

6 Simulation and Experimental Results

The performance of proposed hybrid Topology is simulated using MATLAB/Simulink and tested with the laboratory-based experimental setup. The un-PWM modulation technique is implemented in both simulation and experimental setup. The circuit diagram used in both simulation and experimental setup is shown in Fig. 10 with the corresponding sequence is listed in Table 3.

A new hybrid multilevel inverter embedded with pulse generation scheme of u-n MCPWM techniques is evaluated in both simulation and experimental setup for 13-level inverter. In both simulation and hardware setup, the load values are $R = 120\ \Omega$ and $L = 60$ mH. If the inductor value is high, it will act as a low pass filter and the current waveform shape will be purely sinusoidal. FPGA Spartan controller is used to generate the switching pattern for proposed hybrid topology. The switches IGBTs (BUP400D) and IGBT drivers (HCPL316j) are used in this circuit. The magnitude of each dc source is fixed as 20 V with sum of the 120 V maximum output voltage at the load. Simulated output voltage and current waveform for proposed topology is shown in Fig. 11 with THD results of voltage and current are 5.06% and 2.41% respectively.

The experimental results for hybrid topology are shown in Fig. 12 and 13. The simulation and experimental results have a good agreement in terms of THD for both voltage and current are as 5.270% and 3.18% respectively. Fig. 13 shows the experimental output voltage waveform of proposed hybrid 13-level inverter with peak–peak voltage of 120 V and the maximum current through the load is 1 A.

The power quality analyzer output result and FFT spectrum is shown in Fig. 14 and 15 respectively. The power quality analyzer output result is shown in Fig. 14, which is clearly depicted the rms voltage and current of proposed inverter. Theoretically, the rms output voltage is 84.2 V but in the proposed topology produces, highest rms output voltage of 86.52 V with maximum output power of 54.04 W. In Fig. 15 the FFT spectrum of experimental voltage waveform is presented. The fundamental frequency has maximum magnitude than the other multiple of fundamental frequency. The maximum blocking voltage across the full bridge inverter switches is 80 V and the total maximum blocking voltage across all

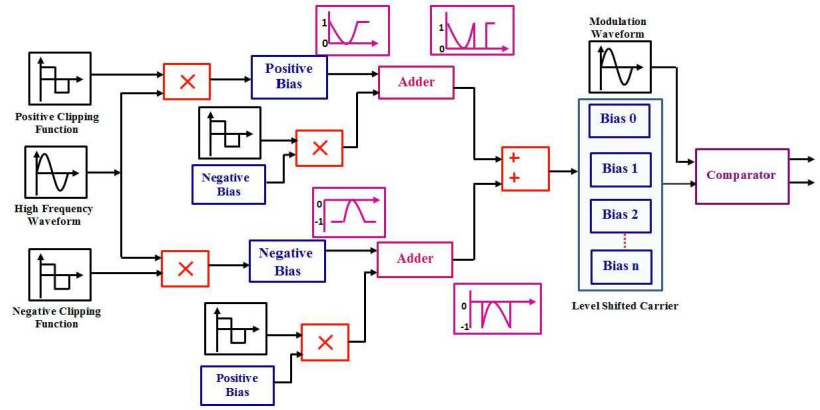


Fig. 6: Scheme of sequential switching of u-n shape carrier modulation technique.

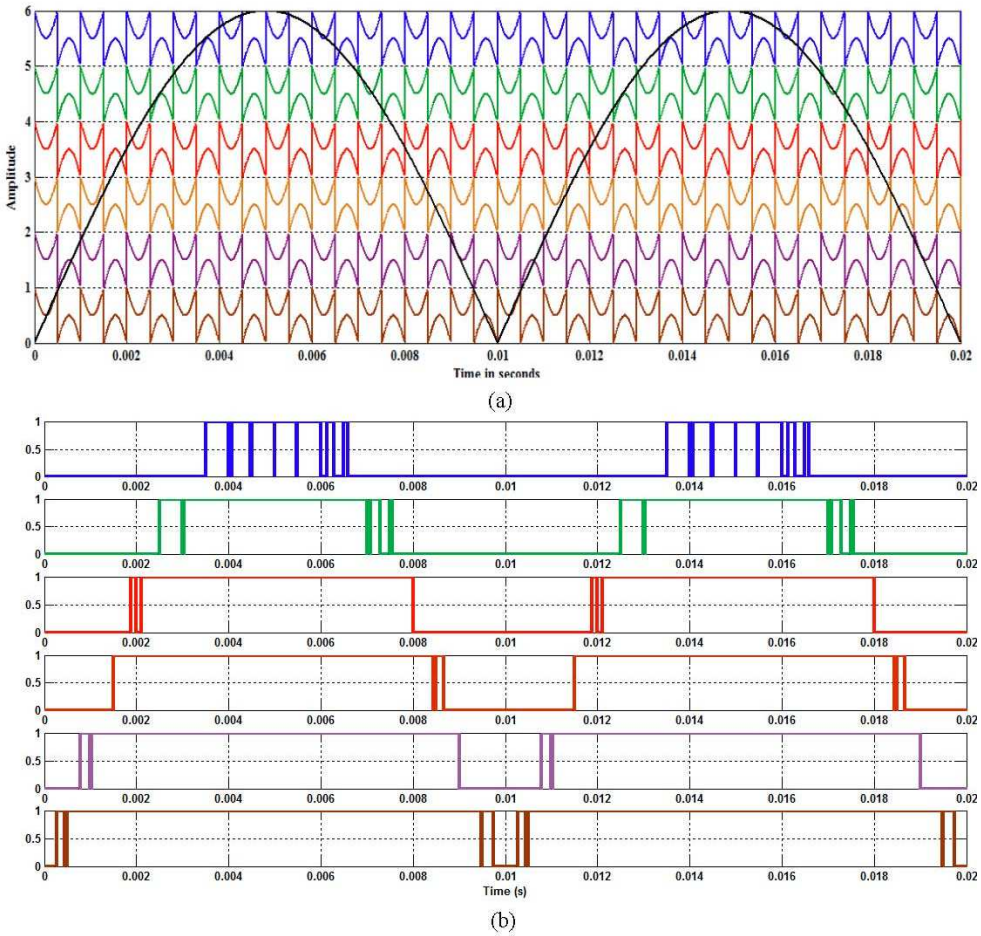


Fig. 7: (a) u-n shaped carrier waveform for 13-Level Inverter and (b) corresponding pulses.

Table 3: Switching pattern for 13-Level topology (ON State).

Level	$S_{11}S_{12}S_1'S_2'S_3'H_1H_2H_3H_4$	Output Voltage
0	(000001100) (001111100) (000000011) (001110011)	0
1	(001111001) (0000001001) (0001000011) (0000010011)	+20 V
2	(001110110) (0000000110) (0001001100) (0000011100)	−20V
3	(100001001) (001010011) (001011100) (001001001) (000011001)	+40 V
5	(100000110) (000110110) (001100110) (000101100) (000100011)	−40 V
⋮	⋮	⋮
12	(111011001)	+120 V
13	(111010110)	−120 V

Table 4: Comparison of proposed modulation technique with other modulation techniques.

References	Modulation Techniques	Switching Frequency	Number of Level	Voltage THD %
[6]	Fundamental Switching Method	–	15-Level	5.82%
[14]	Hybrid Modulation	Upper Cell–10 kHz Lower Cell–50 Hz	13–Level	9.21 %
[15]	PD-MC PWM	4 kHz	15-Level	8.28%
[16]	Fundamental Switching Method	–	15-Level	5.70%
[17]	Fundamental Switching Method	–	17-Level	5.47%
[18]	MCPWM	1 kHz	17-level	6.06%
Proposed	u-n PWM	1kHz	13-Level	5.270%

Table 5: Comparison of power component requirements for 13-Level Inverter with $V_{dc} = 20$ V.

Topology	IGBTs	Gate Driver Circuits	Power diodes	Maximum blocking voltage Except H-Bridge	Maximum Blocking Voltage at H-bridge
CHB Symmetric	24	24	–	20 V	20 V
[9]	9	9	5	20 V	60 V
[10]	16	12	–	60 V	60 V
[11]	18	18	6	20 V	60 V
Proposed	14	14	–	40 V	40 V

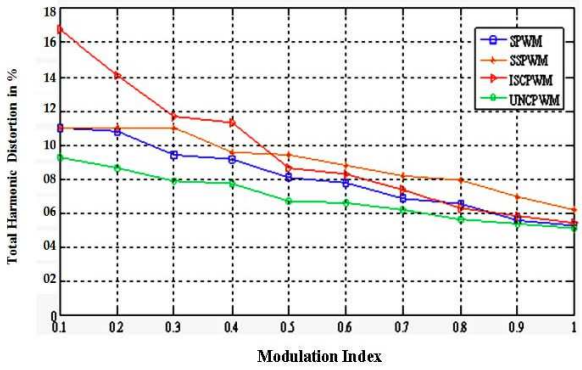


Fig. 8: Total Harmonic Distortion vs. Modulation Index.

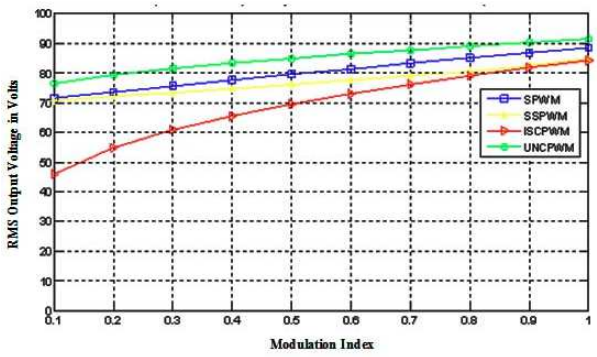


Fig. 9: RMS output voltage vs. modulation Index.

the switches is 600 V for proposed hybrid topology, whereas CHB symmetric uses 24 switches with a maximum blocking voltage of 20 V and the total maximum blocking voltage of 480 V. Here worth mentioned that proposed topology uses half of the CHB topology required. The required number of switches and maximum blocking voltage by switches is listed in the Table 4. In this, resistor and inductor are connected as a series RL load. The isolation circuit and gate circuits are connected together to give better isolation and protection to the FPGA controller.

The voltage THD for different topology and modulation technique is listed in Table 5. It is clear that proposed u-n shape carrier modulation technique is producing low THD with improved RMS voltage of 86.52 V for switching frequency of 1 kHz. Finally, the photograph of prototype model of proposed hybrid multilevel inverter is shown in Fig. 16.

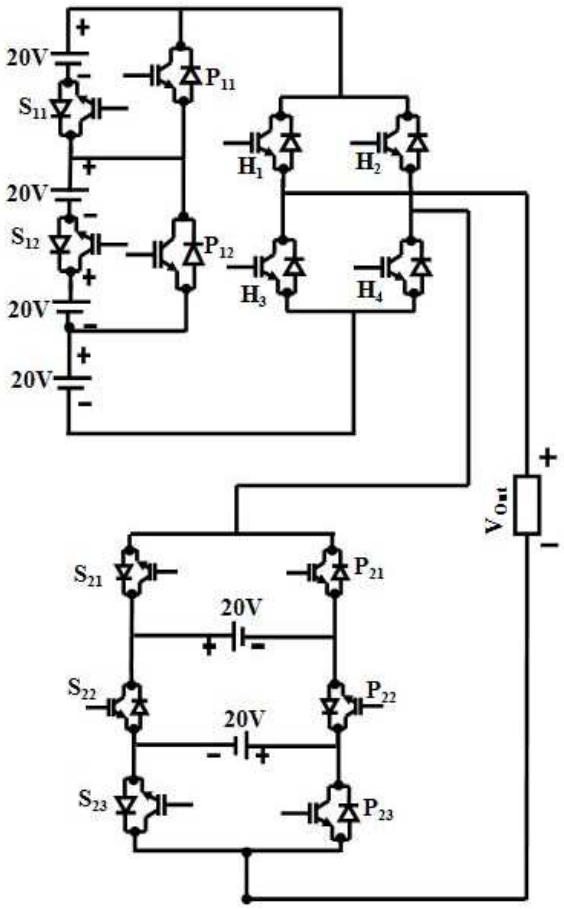


Fig. 10: Circuit diagram of hybrid symmetric topology with basic unit of proposed topology.

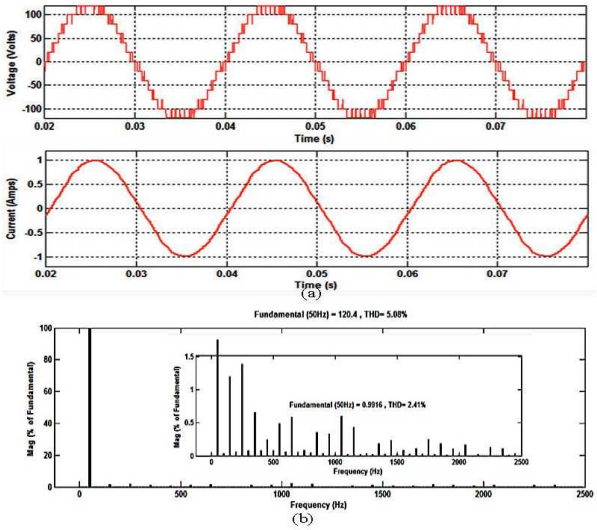


Fig. 11: Simulation results of 13-level inverter (a) voltage and current Waveform (b) Voltage and Current FFT spectrum.

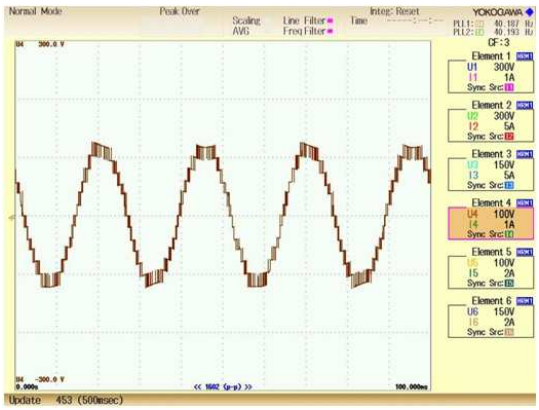


Fig. 12: Experimental results for proposed hybrid topology 13-Level output voltage waveform.

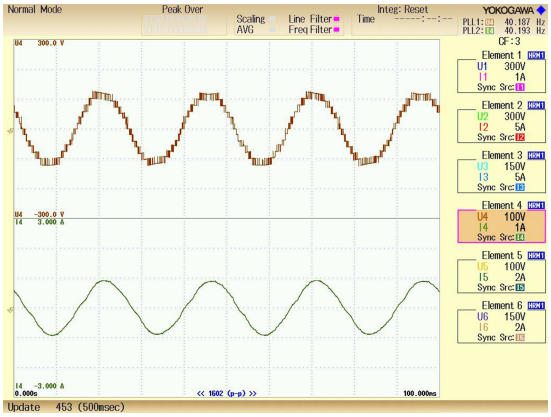


Fig. 13: Experimental results for proposed hybrid topology 13-Level voltage and current waveform.

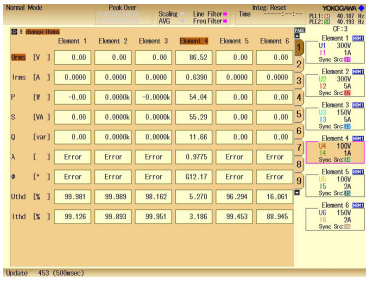


Fig. 14: Power quality analyzer output results.

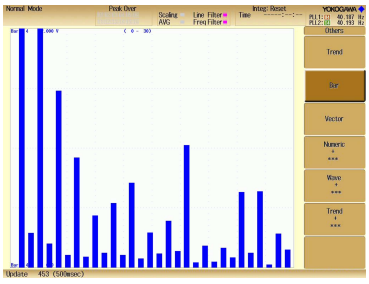


Fig. 15: FFT spectrum of output voltage.

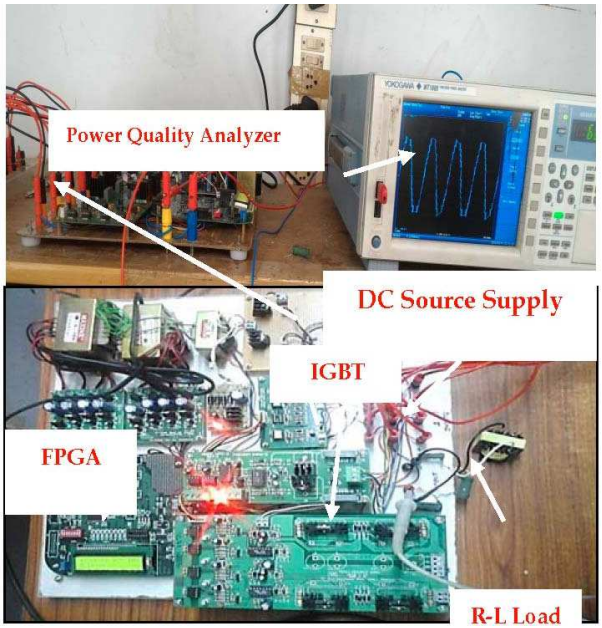


Fig. 16: Photograph of prototype model of proposed hybrid multilevel inverter.

7 Conclusion

In this study, a new hybrid multilevel inverter topology with reduced number of switches and blocking voltage on switches are presented. The blocking voltage on switches in proposed topology is lower than the topology presented in [9–11] but higher than the CHB topology. The number of switches in proposed topology is half of the CHB topology switches which further reduce the switching and conduction losses in proposed topology. To enhance the performance of proposed topology, a new modulation technique is implemented. This modulation technique produces minimum voltage THD (5.270%) with improved RMS voltage (86.52 V) at the load side. A new hybrid topology with u-n shape modulation technique has implemented in laboratory-based test bench and the results are validated.

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