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Analysis of Substrate Coupling in Design of Mixed signal VLSI circuit for 0.18 μm Technology using Resistive Macromodel Method

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Abstract: In this paper the effects of substrate coupling on analog circuits in a mixed-signal chip are described and analyzed based on simulated results. Substrate coupling is a major challenge for mixed-signal design. To analyse the substrate coupling with digital circuits and analog circuit simulation accurate substrate model is important in the modern mixed-signal IC design. At the higher operating frequency the capacitive effect in substrate becomes important and the substrate impedances become frequency dependent in lightly doped substrate. To balance this, heavily doped substrate is used for the analysis and assumed as resistive network. The noise coupling is demonstrated by simulation on 0.18 μm heavily doped CMOS process.

Keywords: Substrate coupling, substrate noise, mixed signal design, output power spectral density.

1 Introduction

Advancement in process technology scaling leading towards one of the major problems in large-scale integration of digital and analog circuits onto a single chip is substrate noise generation and substrate coupling. Digital circuits of is most noisy part of the System-on-Chip, which is responsible for the generation of noise. The noise generated by the digital circuit couples into the sensitive analog and RF circuits through the common substrate. This substrate noise generated by the digital circuit drastically degrades the performance of the analog circuit [1]. Some previous research mainly focused on the sources of substrate noise and substrate noise generation mechanism [2,4,5,6], which are many and complex, and studies have depicted the propagation and effects of substrate noise on analog circuit performance [5,6].

The System-on-Chip has noticeable advantages, but substrate noise coupling becomes very important for mixed-signal designs [1]. The activity of digital switching is produced a pulse shaped current waveform across the power supply lines, this waveform becomes sharper as the technology speed increases and as the number of gates increases the amplitude become larger. As the digital circuit becomes complex and faster the substrate noise produced by the digital circuits become larger, which ultimately degrades the performance of analog circuits integrated on the same die. Various substrate modeling techniques and substrate noise techniques such as the guard rings or the deep trench isolation are already proposed in past researches [2]. To simulate the analog circuit and predict the substrate noise, the main requirement is accurate modeling of the substrate.

The heavily doped substrate behavior at different frequency range changes, so to simulate the analog circuit and model the substrate, a frequency range of interest is required. The substrate coupling through common substrate is seen as resistive at frequency of below GHz frequency [1], and can be modeled as a pure resistive network with multiple ports. If the operating frequency will increase capacitive effect starts arising on the substrate and the impedance of the substrate will become frequency dependent because of the variation conductivities of different doping layers. Moreover in the heavily doped substrate, because of the inductive effect the skin effect will be also an issue in the design [2]. In order to simplify the substrate modeling, the skin effect and the capacitive effect has been separated in this paper.

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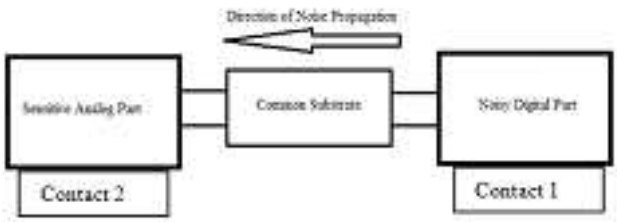

Fig. 1: Representation of Noisy digital section and sensitive analog section integrated on common substrate with separation of *d*

Fig. 2: Substrate profile of heavily doped substrate

A model representation is shown in the Fig. 1; both the digital and analog circuits are integrated on the common heavily doped substrate. The direction of the noise propagation is shown from the digital circuit to analog circuit, and the circuits are integrated at a distance d. The digital and analog circuits are assumed as two contacts separated by a certain distance on the substrate in fig. 2.
This paper is organized as follows. Section II describes the modeling of the heavily doped substrate and equivalent electrical representation. In Section III, explains the system used in the simulation on the basis of the substrate model. In Section IV, the simulation results and the discussion of the results are presented and followed by the conclusion in the Section V.

2 Substrate Modeling

The substrate with heavy doping is shown in fig. 2, and consists of three distinct layers: a heavily doped channel stop implant, a lightly doped epitaxial (epi) layer, and a heavily doped bulk [3]. The width of the different region of substrate profile and resistivity is given. The backplane of the substrate region is having width and length of 800μm and the backplane is grounded. For the analysis purpose, two contacts, each contact having the width and length of 10μm and thickness of 0.28 μm with a separation of 60 μm is place on the top of the substrate. These two contacts are modeling the digital and analog circuits of the mixed signal system. The main motive of this substrate modeling is to analyze the coupling between the contacts on the different frequency of operation, and can be use in the analog circuit simulation and substrate noise estimation for the mixed signal design.
In Fig. 2, the cross section of a typical heavily doped substrate is shown. The digital circuit is represented as source contact and analog circuit is represented as sensor contact. The coupling between the source and sensor contact can be determine by using device simulator. The macro model of the contacts for the heavily doped substrate and the equivalent circuit is given in fig.3. For frequencies up to Gigahertz and below, the substrate can be treated as a lumped resistive network [1,8]. The resistance between the source contact and sensor contact to the bulk are $R_{11}(G_{1A}=1/R_{11})$ and R_{22} $(G_{1B}=1/R_{22})$ respectively, and the resistance for the cross coupling is represented by $R_{12}(G_2=1/R_{12})$. As the separation between the contacts increases the value of the R_{12}will increases, i.e. for small separation the value of R_{12} will be small.
In order to obtain a Y-parameter matrix for the equivalent circuit of the heavily doped substrate, an ac voltage is applied at one port and the currents are measured with other port connected to ground. Assume that sizes and shapes of the contacts are the same, then it gives: G_{11} = G_{22} = G_{12}. The following two-port Y-parameters for the substrate macromodel is shown:

$$Y = \begin{bmatrix} y_{11}\, y_{12} \\ y_{21}\, y_{22} \end{bmatrix} = \begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_1 + G_2 \end{bmatrix} \quad (i)$$

In order to determine G1 and G2, a Z-parameter matrix is used, and it gives:

$$Z = \begin{bmatrix} z_{11}\, z_{12} \\ z_{21}\, z_{22} \end{bmatrix} = Y^{-1} = \frac{1}{G_1^2 + 2G_1G_2} \begin{bmatrix} G_1 + G_2 & G_2 \\ G_2 & G_1 + G_2 \end{bmatrix}$$

(ii)

Let $\delta = (G12 + 2G1G2)$ be the determinant of the Y-parameter matrix. Z_{11} is a constant ξ because it is the impedance of contact one to the substrate, with all other contacts flowing. Thus, the constant ξ can be extracted from simulations. This gives

$z_{11} = \frac{G_1+G_2}{G_1^2+2G_1G_2} = \xi \quad => \quad G_1^2 + 2G_1G_2 - \frac{1}{\xi}(G_1 + G_2) = 0$ *(iii)*

Rearranging the above equation,

$$G_1(x) = \frac{1}{2\xi} - G_2(x) + \frac{1}{2\xi}\sqrt{1 + 4\xi^2 G_2^2(x))}$$

(iv)

where G1 and G2 can be determined from simulators and measurements, and they are dependent of the separations between the source and sensors. Based on the linear dependence on the semi-plot of G2, it provides a relationship between G2 and the separation d.

$$G_2(x) = \alpha e^{-\beta d} \quad (v)$$

Table 1: substrate resistance for heavily doped substrate

Separation (μm)	*R11* (Ω)	*R22* (Ω)	*R12* (Ω)
15	392	390	960
30	310	310	33.8K
90	305	305	2.58M

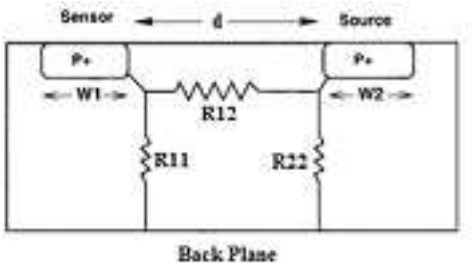

Fig. 3: Substrate resistive macromodel for the heavily doped susbtrate

where α and β are constants determined from simulations and measured data.

Consequently, there are only two contact points required to obtain relatively accurate results, so the accuracy of α and β can be improved with more data and a nonlinear least-square fit. The main shortcoming of this method is that it can only be used on the heavily doped substrate. Moreover, the operating frequency must be below GHz because the substrate can only be modeled as the equivalent circuit as illustrated in Fig. 3.

Practically the contact may be different shape and size in design of integrated circuit. To extracting the substrate resistance scalable model with the separation is important. The variation of resistance between the contacts, between the contact and backplane with the separation of contact can be determined by the simulation. Resistor values for two identical contacts at various separations in a heavily doped substrate is given in table-I. If the contacts are same in size then the resistance between the contact and backplane for both contacts will be almost equal.

$R_{11}=R_{22}$ *(vi)*

If the separation between the contacts is increasing the resistance between the contacts will increase. At the large separation the resistance value will be very large in order of $M\Omega$ and the current generated by the noise source will flow in to the substrate through the resistance between the contact and backplane, if the backplane if not grounded. This current again back to the analog circuits and degrade the performance of the same. At large separation between the digital and analog circuit about 90 μm results only a negligible improvement in the substrate coupling.

The substrate is modeled by a two-port lumped resistor network and it is valid for frequencies below Gigahertz frequency. The substrate coupling model used in this

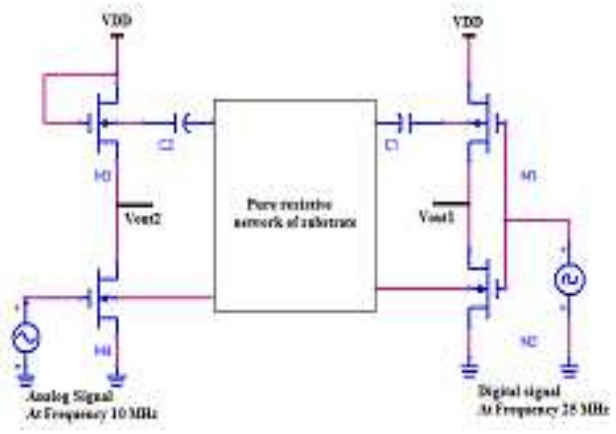

Fig. 4: Circuit representation of contact to analyze substrate coupling

work is scalable with contact separations. The lumped resistive model for to contacts and to contacts is shown in Fig. 3. Typical values of the R_{11}, R_{12} and R_{22} are function of spacing between the contacts and the values are given for the $0.18\mu m$ technology is given in the table I. the values of the resistors are not depending upon the size of the contacts. Both R_{11} and R_{22}resistances are approximately constant and independent of the separation for the same size of the contacts. For a larger separation between the digital and analog contacts the value of R_{12} is very high.

3 Systems and Simulation

To demonstrate the substrate coupling in a practical circuit, the contacts discuss in previous section now implemented as two different circuits connected with resistive network. The two circuits acts as two different contacts and the connecting resistive network is as pure resistive substrate network. The circuit representation to analyze the substrate coupling is shown in Fig.4.

The substrate coupling is analyzed with a CMOS inverter connected with saturated load n-MOS inverting amplifier through a resistive network, design with 0.18 m technology. The separation between the CMOS inverter and the saturated load inverter is kept fix. The substrate resistive

model is derived for the two amplifiers. The value of the resistances is obtained by the *n*-port impedance matrix, constructed from two port impedance matrix. The circuit representation of the setup used is shown in Fig. 4 whereas the resulting resistive substrate coupling network is shown in Fig. 5. In the circuit of Fig. 4, C_1 and C_2 are the n-well–substrate capacitances that are not included in circuit simulation.

The resistors in resistive network in fig. 5, resistors R_{12}, R_{13}, R_{14}, R_{23}, R_{24}, *and* R_{34} represent the resistances

Table 2: COMPARISON BETWEEN DIFFERENT SUBSTRATE MODELING TECHNIQUE

Techniques	Accuracy	Difficulty	Simulation Time	Generality	Assumption made
Finite Difference Method	Good depends highly on the resolution of discretization	Hard large mesh matrix size	Long huge matrix sparse size	lightly and heavily doped substrate	consisting of purely resistive mesh
Boundary Element Method	Excellent within 10% of the actual answer	Hard cumbersome mathematics	Quite Long DCT can be used as an efficient solver.	lightly and heavily doped substrate	constant current density across a port
Resistive Macromodels Method	Good improved by more input data	Simple only 3 parameters (α, β, ξ) required	Short	heavily doped substrate	treated as a resistive network for low frequency

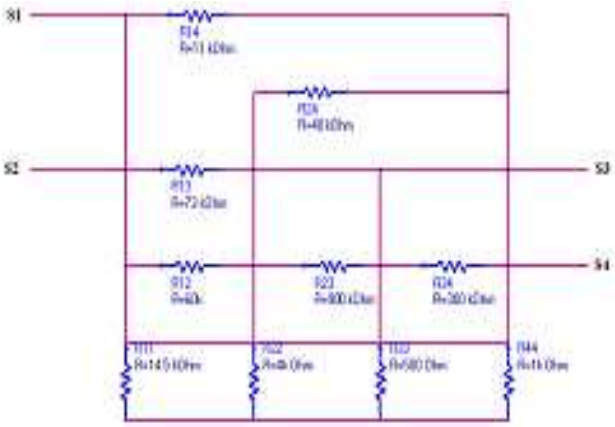

Fig. 5: Resultant substrate network for the prediction of substrate coupling

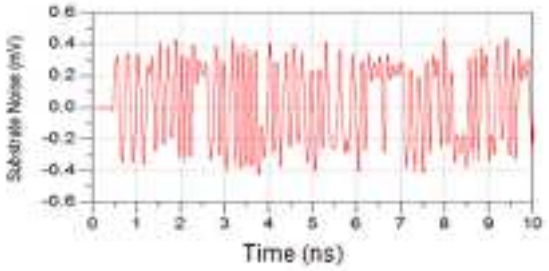

Fig. 6: Simulated substrate noise waveform at the output of the amplifier.

between contacts while resistors R_{11}, R_{22}, R_{33}, *and* R_{44} represent the resistances between the contacts and the back plane. The separations between the contacts are important for the calculation of the value of resistances and are calculated by the layout design rules and transistor size. Since noise coupling through the substrate is important so the power supply inductances are no considered in the simulation.

To analyze the substrate coupling between the circuits in fig. 4, a square pulse of frequency 25 MHz is applied to the CMOS inverter and a sinusoidal signal input of frequency 10 MHz is applied to the saturated load inverting amplifier. The pulse frequency is chosen enough larger than frequency of sinusoidal signal, that no harmonics of sinusoidal lie in the range of the pulse frequency in output spectrum. The pMOS transistor was chosen to be approximately twice as big as the nMOS transistor for 0.18m technology.

4 Results Discussion

A time domain simulation is done for the circuit, and substrate noise waveform is shown in fig. 6 at the output of the saturated load inverting amplifier.

The output power spectral density of the saturated load inverting amplifier is shown in fig. 7, when no input is applied to the CMOS inverter (no digital block). When no pulse input is applied to the CMOS inverter and the separation between the circuits is the order of 10 μm, no coupling is seen in the output power spectral density at the output of the amplifier output. When no input is

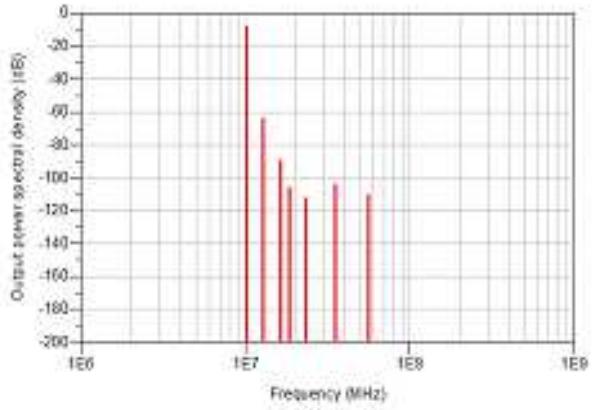

Fig. 7: Output power spectral density at the output of the amplifier at 10 MHz with no input at digital CMOS

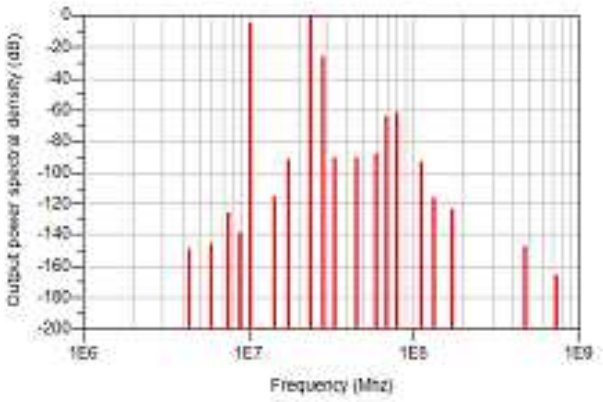

Fig. 8: Output power spectral density at the output of the amplifier at 10 MHz with input at digital CMOS of frequency 25MHz

applied to the digital CMOS inverter only a peak at 10 MHz is appeared in output power spectral density, which is due to the input and some harmonics resulting from the amplifier design.

When the digital CMOS inverter is place nearby and a square pulse of frequency 25 MHz is applied to it, then in this case amplifier shows two peaks at output. One at the 10 MHz and other is 25 MHz with associated harmonics, in the output power spectral density at the output of the amplifier and shown in the fig 8. This is representing the substrate coupling of the digital signal. The phenomenon of the substrate coupling is appeared at the contact separation of the order of $15\mu m$ to $20\mu m$.

It is confirming the coupling of the digital noise and the amplifier output is dominated by the substrate coupling for this small separation of $15\mu m$.

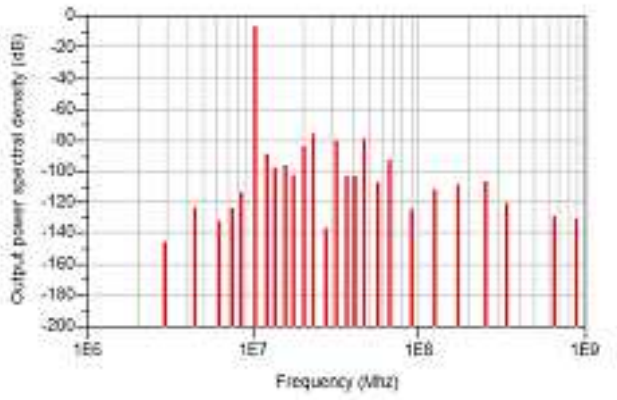

Fig. 9: Output power spectral density at the output of the amplifier at 10 MHz with input at digital CMOS of frequency 25MHz (when separation is 90m)

The same circuit is simulated with the increased circuit separation of the order of $90\mu m$, as the separation between the amplifiers and increased to $90\mu m$; a significant attenuation is shown by the amplifier output at 25 MHz in the output power spectral density. Which is depicting that isolation between the circuits is increased shown in fig 9.

5 Conclusions

The substrate noise coupling is analyzed and simulated using the 0.18 μm technology up to Gigahertz frequency or lower using the scalable model of substrate with separation between the digital and analog circuits for heavily doped substrate. The effect of substrate noise coupling on analog circuit, in presence of digital circuit is discussed at different separation between the circuits. At lower separation the substrate coupling is dominating the performance of the analog circuit but at larger separation isolation is increased between the contacts and the substrate coupling is not prominent. As the separation is increasing after this point, it will not having significant impact on the substrate coupling.

References

[1] Anil Samavedam, Aline Sadate and Kartikeya Mayaram," A Scalable Substrate Noise Coupling Model for Design of Mixed-Signal IC's" *IEEE journal of solid-state circuits*, vol. 35, no. 6, pp 895-904, june 2000.

[2] Zhuoxiang Ren, Hazem Hegazy, and Nur Kurt-Karsilayan "Characterization of Dynamic Substrate Macro-Model in Mixed Signal IC Systems Using 3-D Finite Element Method" *IEEE transactions on magnetics*, vol. 44, no. 6, pp 1466-1469, June 2008.

[3] Jim Le, Christopher Hanken, Martin Held, Michael S. Hagedorn, Kartikeya Mayaram, "Experimental Characterization and Analysis of an Asynchronous Approach for Reduction of Substrate Noise in Digital Circuitry" *IEEE transactions on very large scale integration (vlsi) systems*, vol. 20, no. 2, pp- 344-356, February 2012.

[4] Brian E. Owens, Sirisha Adluri, Patrick Birrer, Robert Shreeve, Sasi Kumar Arunachalam and Kartikeya Mayaram "Simulation and Measurement of Supply and Substrate Noise in Mixed-Signal ICs" *IEEE journal of solid-state circuits*, vol. 40, no. 2, pp 382-391, february 2005

[5] N. K. Verghese, D. J. Allstot, and M. A.Wolfe, "Fast parasitic extraction for substrate coupling in mixed-signal ICs," *IEEE Custom Integrated Circuits Conf.*, pp. 121–124, 1995.

[6] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE J. Solid-State Circuits*, vol. 31, pp. 344–352, Mar. 1996.

[7] J. P. Costa, M. Chou, and L. M. Silveira, "Efficient techniques for accurate modeling and simulation of substrate coupling in mixed-signal IC's," *IEEE Trans. Comput.-Aided Des.*, vol. 18, no. 5, pp. 597–607, May 1999.

[8] T. Smedes, N. P.Van Der Meijs, and A. J. van Genderen, "Extraction of circuit models for substrate cross-talks," in *IEEE/ACM Int. Conf. CAD Dig. Tech. Papers*, 1995, pp. 199–206.

[9] B. R. Stanisic, N. K. Verghese, R. A. Rutenbar, R. L. Carley, and D. J. Allstot, "Addressing substrate coupling in mixed-mode IC's and power distribution synthesis," *IEEE J. Solid-State Circuits*, vol. 29, pp. 226–237, Mar. 1994.

[10] N. K. Verghese, T. J. Schmerbeck, and D. J. Allstot, *Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits*. Norwell, MA: Kluwer, 1995.

[11] E. Charbon, R. Gharpurey, R. G. Meyer, and A. Sangiovanni-Vincentelli, "Substrate optimization based on semi-analytical techniques," *IEEE Trans. Computer-Aided Design*, vol. 18, pp. 172–190, Feb. 1999.

[12] M. Badaroglu, M. van Heijningen, V. Gravot, J. Compiet, S. Donnay, G. G. E. Giellen, and H. J. De Man, "Modeling and experimental verification of substrate noise reduction in CMOS mixed-signal IC's with synchronous digital circuits," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1383–1395, Nov. 2002.

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