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P-Channel Gd_2O_3 Trapping Layer for SONOS-Type Flash Memory

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Abstract: This paper proposes and demonstrates a p-channel SONOS-type memory based on a high-κ dielectric material gadolinium oxide (Gd_2O_3) trapping layer. In the proposed design, we used band-to-band hot electron injection for programming, and channel hot-hole injection for erasing through a highly efficient charge storage device operation. The proposed design has a total memory window of $11V$, 10-year V_t retention window with approximately 9% charge loss, and sufficient memory window for 104 programming/erasing cycles of endurance. The proposed p-channel SONOS-type Gd_2O_3 trapping layer flash memory exhibits large memory windows, high program/erase speed, excellent endurance, and optimal disturbance characteristics.

Keywords: Flash memory, gadolinium oxide, nonvolatile memory, p-channel

1 Introduction

Flash memories are widely applied to digital cameras, tablet PCs, and smart phones as a portable mass storage. A crucial challenge in the electronics industry is obtaining nonvolatile low-powered fast memories with short dimensions. Conventional floating gate (FG) memory devices encounter problems with scaling down because they use a thick tunneling oxide to guarantee a long charge retention time for continuous charge storage [1,2,3,4,5]. Upon scaling the tunneling oxide thickness down, the FG easily loses charge due to defect generation caused by program/erase cycles or direct current tunneling [6].

A SONOS-like (silicon-oxide-nitride-oxide-silicon) structure including nitride memories and nanocrystal memories for charging devices has recently become attractive because it does not have a planar scaling problem for floating gate isolation and exhibits considerable potential for achieving high program/erase speed, low programming voltage, and low power performance [6,7,8,9,10,11,12,13,14,15,16,17].

Recently, n-channel flash memories have been used in the design of flash memory products. However, the high voltage operation results in large power consumption through channel-hot-electron (CHE) programming. Therefore, the p-channel flash memory device using band-to-band tunneling-induced hot electron injection (BBHE) was proposed [18,19,20]. For the comparison with n-channel flash memory device, p-channel flash memory devices offer several advantages, such as lower power consumption, higher program/erase speed, and superior reliability.

Several recent studies presented various types of high-κ dielectric trapping layers as potential candidates for replacing Si_3N_4 to provide discrete charge storage in nonvolatile memory [21,22,23,24,25,26]. Furthermore, high-κ dielectric materials can improve the gate capacitance, and maintain an equivalent potential difference for a greater thickness compared to SiO_2. Therefore, the leakage through the dielectric can be minimized, and the scaling limits can be extended. Moreover, to achieve a large memory window for differentiating between stable program and erased states, high-κ dielectric trapping layer can provide sufficiently high trapping density for charge storage [27,28].

Using the high-κ trapping layer for flash memory exhibits several advantages, for example, easy fabrication, high program/erase speed, low program/erase operation voltage, power consumption, and higher potential for scalability below the 40-nm node according to the International Technology Roadmap for Semiconductors (ITRS) [29].

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Rare earth oxides, such as Gd_2O_3, are attractive candidates for trapping layer memory because of their thermodynamic stability consideration, high dielectric constant, proper conduction, and valence band offset with Si, low lattice mismatch with silicon, and excellent electrical properties [30,31,32]. High trapping state densities can improve the charge-trapping efficiency, and ultimately achieve a larger operation window. This makes it possible to further reduce the operation voltage and potentially improve memory device scaling.

The experiments in this study fabricated a high-performance p-channel nonvolatile memory with a high-κ material gadolinium oxide (Gd_2O_3) charge-trapping layer. The proposed design exhibited excellent characteristics regarding a considerably large memory window, high-speed program/erase, excellent endurance, and optimal disturbance.

2 Experimental

Fig. 1 schematically depicts the device structure and process flow of the proposed flash memory. The fabrication process of the p-channel Gadolinium oxide memory devices began with a LOCOS isolation process on n-type, $5-10\Omega cm$ (100), $150mm$ silicon substrates.

First, a 3-nm-thick tunnel oxide was thermally grown at $1000^{\circ}C$ in a vertical furnace system. A 5-nm-thick Gadolinium oxide layer was subsequently deposited by the E-gun method with Gadolinium oxide targets. The samples subsequently underwent RTA treatment in N_2O ambient at $900^{\circ}C$ for 1 min. A blocking oxide approximately 10-nm-thick was subsequently deposited by high-density plasma chemical vapor deposition (HDPCVD), followed by a 1 min, $900^{\circ}C$ N_2 densification process.

A 200-nm-thick poly-Si layer was subsequently deposited by LPCVD to serve as the gate electrode. The gate electrode was patterned, and the source/drain (S/D) and gate were doped with self-aligned BF_2 ion implantation at a dosage and energy of $5x10^{15} ions/cm^{-2}$ and $20KeV$, respectively. The substrate contact was patterned, and the sub-contact was implanted with phosphorous at a dosage and energy of $5x10^{15} ions/cm^{-2}$ and $40KeV$, respectively. After these implantations, the dopants were activated at $950^{\circ}C$ for $20s$. Standard CMOS procedures were subsequently completed to fabricate p-channel Gadolinium oxide high-κ memory devices.

3 Results and Discussion

For the operation of the proposed p-channel Gd_2O_3 trapping layer flash memories, we used band-to-band hot-electron injection and channel hot-hole injection for the programming and erasing, respectively. All devices described in this paper had dimensions of $L/W = 2/2\mu m$.

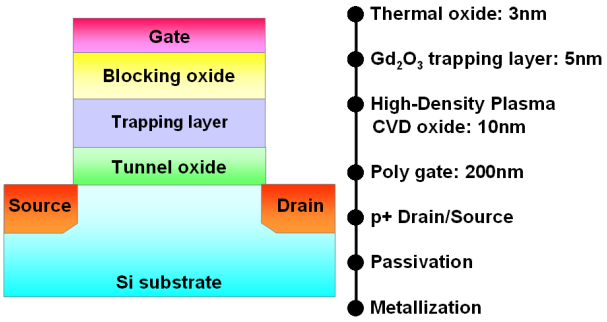

Fig. 1: P-channel Gd_2O_3 flash memory cross-section cell structure and process flow of the proposed flash memory cell.

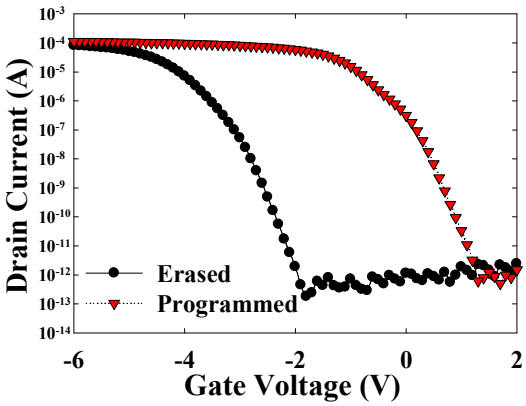

Fig. 2: I_{DS}-V_{GS} characteristics of P-Channel Gd_2O_3 memory devices.

Fig. 2 shows the Ids-Vgs curves of the p-channel Gd_2O_3 trapping layer memory devices with programming time of $1ms$ and erasing time of $0.1ms$. Band-to-band hot-induced electron (BTBHE) and channel hot hole (CHH) were employed for programming and erasing, respectively. Both source and substrate terminals were biased at $0V$. The $V_t shift$ is defined as the threshold voltage change of a device between the written and the erased states. A relatively large memory window of about $4V$ can be achieved. (Programming conditions: $V_g = 8V$, $V_d = -10V$ for $0.1ms$; erasing conditions: $V_g = -10V$, $V_d = -11V$ for $1ms$.)

Fig. 3 shows the program speed of the p-channel Gd_2O_3 flash memory. We used band-to-band hot-induced electron (BTBHE) to the program, and the program conditions were 1) $V_g = 6V$, $V_d = -7V$, 2) $V_g = 7V$, $V_d = -8V$, and 3) $V_g = 8V$, $V_d = -10V$. The program speed can be as fast as $0.1ms$ with a $4.1V$ memory window for program condition $V_g = 8V$, $V_d = -10V$. As shown in Fig. 3, the V_{th} shift increases in conjunction with the applied gate voltage. This occurred because a larger applied gate voltage generates a greater number of hot electrons. More electrons are able to cross the barrier

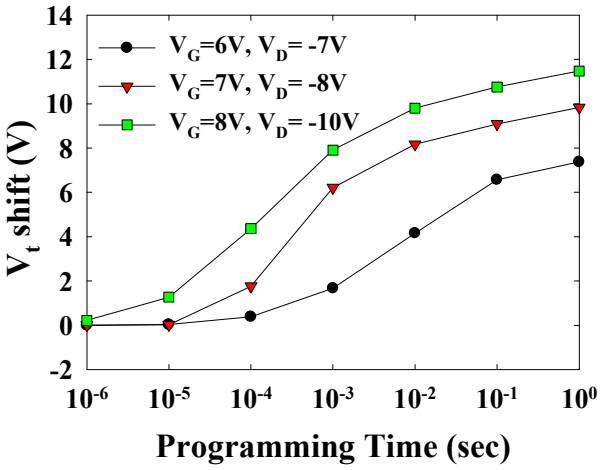

Fig. 3: Program characteristics of the p-channel Gd_2O_3 flash memory devices with various programming conditions.

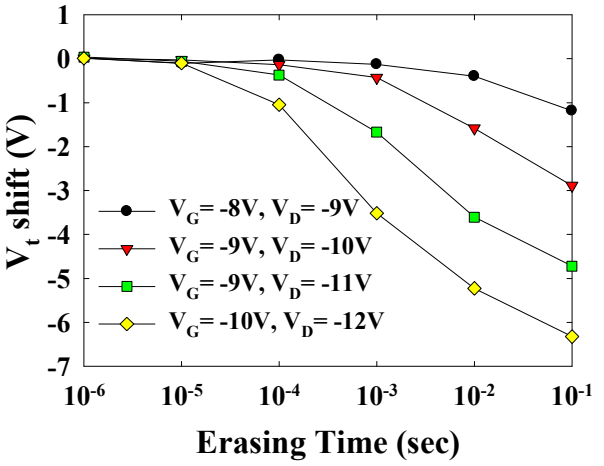

Fig. 4: Erase characteristics of the p-channel Gd_2O_3 flash memory devices with various erasing voltages.

height and are trapped in the Gd_2O_3 trapping layer; therefore, the V_{th} shift increases.

The erase speed of the p-channel Gd_2O_3 flash memory is also demonstrated in Fig. 4. We used channel hot hole (CHH) to erase, and the erase conditions were as follows: 1) $V_g = -8V$, $V_d = -9V$, 2) $V_g = -9V$, $V_d = -10V$, 3) $V_g = -9V$, $V_d = -11V$, and 4) $V_g = -10V$, $V_d = -12V$. The normalized erase speed curve appears in Fig. 4, and the same explanation can be applied on the V_{th} shift as the gate voltage increases in negativity. The use of BTBHE to program and CHE to erase can yield high program/erase efficiency.

Fig. 5 illustrates the retention characteristics observed at temperatures of $25°C$ and $85°C$, and under 10 000 P/E (program/erase) cycles device at $85°C$. At room temperature and at a high temperature of $85°C$, the charge

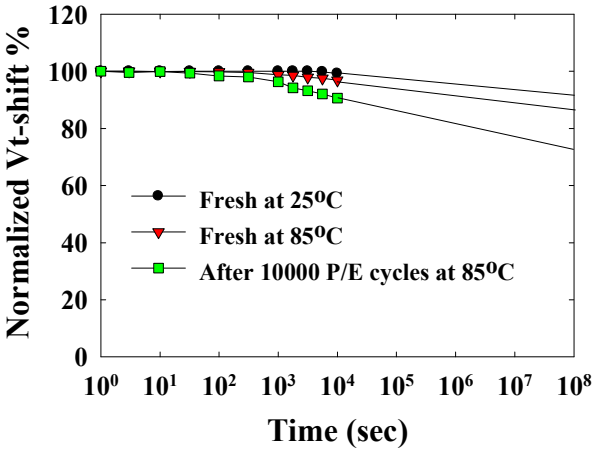

Fig. 5: Retention characteristics of p-channel Gd_2O_3 flash memory devices at temperatures of $25°C$ and $85°C$, and under $10000P/E$ (program/erase) cycles device at $85°C$.

loss of the p-channel Gd_2O_3 flash memory was below 9% and 14%, which is an estimation based on an extrapolation at 108 s. This behavior may be closely related to the trap energy level in high-κ dielectrics [27]. For the 10 000 P/E cycles device at a temperature of $85°C$, we observed a considerable charge loss of approximately 28%, which is an estimation based on an extrapolation at $108s$. This strong temperature dependence was predictable from the large activation energy; however, the detailed mechanism remains under investigation.

Fig. 6 displays the endurance characteristics after $105P/E$ cycles (programming conditions: $V_g = 8V$, $V_d = -10V$ for $0.1ms$; erasing conditions: $V_g = -10V$, $V_d = -11V$ for $1ms$). A slight memory window narrowing occurred, and the individual threshold voltage shifts became visible in the program and erase states after 102 cycles. This finding suggests the formation of operation-induced trapped electrons [33]. This feature is closely related to the use of the thin tunnel oxide and the minute amount of residual charge remaining in the tunnel oxide and Gd_2O_3 layer after cycling. After $104P/E$ cycles, the memory window for distinguished charge storages was fixed at approximately $1.7V$. This finding suggests that the p-channel Gd_2O_3 flash memory can be a candidate for the SONOS-like memory application.

Fig. 7 displays the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for cells sharing a common word-line when one of the cells is being programmed. We observed a threshold voltage shift of only $0.1V$ under the following conditions: $V_g = 10V$; $V_s = V_d = V_{sub} = 0V$; stressed for $1000s$. Two possible causes are proposed for small gate disturbance. First, when a flash cell is programmed by Fowler-Nordheim tunneling (FN tunneling), electron injection from the floating gate resulting in electron-hole

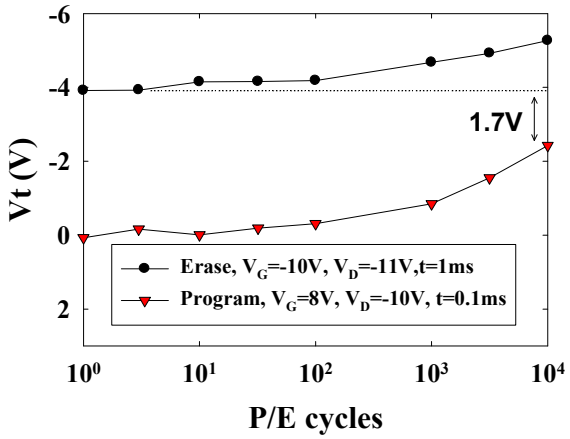

Fig. 6: Endurance characteristics of p-channel Gd_2O_3 flash memory devices after $104P/E$ cycles.

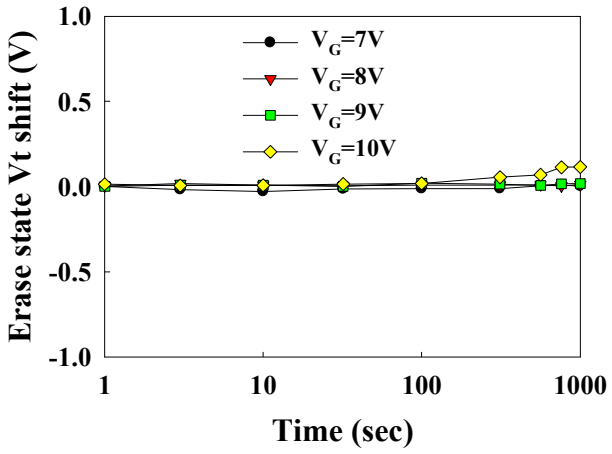

Fig. 7: Gate disturbance characteristics of p-channel Gd_2O_3 flash memory devices: A threshold voltage shift of $0.1V$ occurred after stressing at $V_g = 10V$ and $V_s = V_d = V_{sub} = 0V$ for $1,000s$.

pairs by impact ionization occurred at the Si-SiO_2 interface. For the p-channel device, the programmed electron is the minority carrier of the part of n-type substrate, and a lower amount of electrons is injected and trapped into the oxide. Therefore, the gate disturbance of the p-channel flash device is superior to that of the n-channel flash device. Second, because of the small voltage drop at the tunnel oxide when using the serial capacitor voltage divider model, this memory exhibits excellent gate disturb characteristics, even with such a thin tunnel oxide.

Fig. 8 presents the programming drain disturbance of the proposed p-channel Gd_2O_3 trapping layer SONOS-type memory. Three distinct drain voltages ($V_d = -10$, -11, and $-12V$) were applied in the programming drain disturbance measurements at room temperatures. We observed that a sufficient programming

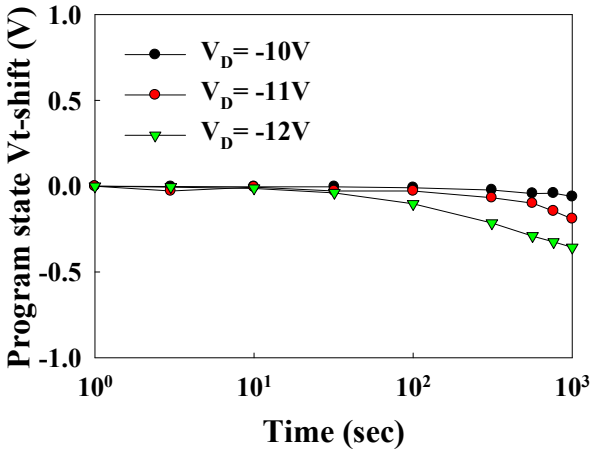

Fig. 8: Drain disturbance characteristics of the p-channel Gd_2O_3 flash memory cells: A sufficient programming drain disturbance margin exists ($\Delta V_t < 0.5V$) after programming at a value of V_d of $-12V$ at room temperature.

drain disturb margin exists ($\Delta V_t < 0.5V$), even after programming at a value of V_d of $-12V$ under room temperature, and after stressing for $1000s$. Fig. 9 demonstrates the read disturbance-induced erase-state threshold voltage instability in a p-channel-localized Gd_2O_3 trapping storage flash memory cell under several operation conditions. For two-bit operation, the applied bit-line voltage in a reverse-read scheme must be sufficiently large ($> -2V$) to permit a read through of the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors, that is, the word-line and the bit-line. The word-line voltage during reading may enhance the room-temperature drift in the neighboring bit [34,35,36]. Conversely, a relatively large read bit-line voltage may cause unwanted channel hot-hole injection, and subsequently result in a considerable threshold voltage shift of the neighboring bit. In our measurements, the gate and drain biases were applied, and the source was grounded. The results demonstrate that almost no read disturbance occurred in the proposed p-channel-localized Gd_2O_3 flash memory under low-voltage reading ($V_g = -2V$; $V_d = -2.5V$). For a larger memory window, we discovered that only a small read disturbance (approximately $0.1V$) occurred after operation at a value of Vd of $-3V$ for $1000s$ at $25^{\circ}C$.

Table 1 summarizes the bias conditions for two-bit operation. We programmed the Bit1 and Bit2 with the bias condition of $V_d = -10V$ and $V_g = 8V$ with the programming time of $0.1ms$, and erased the Bit1 and Bit2 with the bias condition of $V_d = 10V$ and $V_g = -10V$ with the erasing time of $1ms$. The read operation was achieved using a reverse read scheme with $V_d = -3V$ and $V_g = -2V$. The depletion regions of drain side and source side are able to mask the effect of the stored charge. Therefore, We employ forward and reverse reads to detect

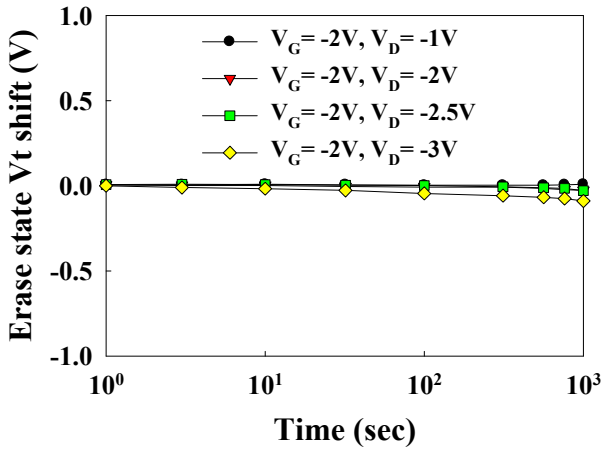

Fig. 9: Read disturbance characteristics of the p-channel Gd_2O_3 flash memory: A slight V_t shift occurred for $V_d = -3V$, after $1,000s$ at $25°C$.

Table 1: Operating principles and bias conditions utilized during the operation of the p-channel Gd_2O_3 flash memory.

		Program	Erase	Read
Bit 1	V_G	$8V$	$-10V$	$-2V$
	V_D	$-10V$	$-11V$	$0V$
	V_S	$0V$	$0V$	$< -3V$
Bit 2	V_G	$8V$	$-10V$	$-2V$
	V_D	$0V$	$0V$	$< -3V$
	V_S	$-10V$	$-1V$	$0V$

the information stored in the programmed bit 1 and bit 2, respectively.

Table 2 presents a comparison of our results with those of recent investigations into new devices [13,21,25, 37]. Our system shows a number of salient features. First, our p-channel Gd_2O_3 flash memory exhibit larger memory windows than do the other systems because of the large trap density of the high-κ dielectric materials. Second, we observed good retention with localized charge storage by using high-κ dielectric materials as the trapping layer. Third, with respect to the P/E speed, we obtained a high speed of operation because we used band-to-band hot-electron programming and channel hot-hole erasing for the p-channel devices. Finally, we have enough memory window of our p-channel Gd_2O_3 flash memory for distinguished charge storages after $104P/E$ cycles. These advantages suggest that the p-channel Gd_2O_3 flash memory can be a candidate for the SONOS-like memory application in the future.

4 Conclusions

This study investigated the effect of memory on the performance of p-channel Gd_2O_3 SONOS-type flash memory. The proposed design exhibited excellent characteristics regarding large memory windows, high-speed program/erase, excellent endurance, and optimal retention for device operation. Small voltage shift of gate disturbance, drain disturbance, and read disturbance characteristics can be achieved. Hence, Gd_2O_3 may be a candidate material for the trapping layers of p-channel SONOS-type memory.

Table 2: Comparison of memory characteristics of this work to the most recent works on SONOS-type memory devices

	Memory windows (volts)	20% charge loss (sec)	P/E speed (sec)	Endurance
This Work	$11V$	$> 10^8$	$P :> 10^{-5}$ $E :> 10^{-4}$	$> 10^4$
HfO_2 [25]	$7V$	$> 10^5$	$P :> 10^{-5}$ $E :> 10^{-5}$	$> 10^5$
Si dots [37]	$2.2V$	$> 10^6$	$P :> 10^{-6}$ $E :> 10^{-1}$	$> 10^4$
Metal dots [13]	$7V$	$> 10^4$	$P :> 10^{-3}$ $E :> 10^{-3}$	$> 10^7$
SONOS [21]	$5.2V$	$> 10^8$	$P :> 10^{-6}$ $E :> 10^{-5}$	$> 10^6$

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