International Journal of Thin Films Science and Technology
An International Journal

Influence of thickness and annealing temperature on structural and electrical properties of Te/Si heterojunction

Mahdi H. Suhail*, Souad G. Kaleel and Marwa R. Fahad**

***Dept. of Physics, College of Science for women, Univ. of Baghdad*
**Dept. of Physics, College of Science, Univ. of Baghdad*
E Mail:mhsuhail@yahoo.com

Received: Jan. 18, 2012; Revised March 4, 2012; Accepted April 26, 2012
Published online: 1 May 2012

Abstract: Heterojunctions are fabricated by depositing tellurium films on n-type single (n-Si) wafers by the method of vacuum evaporation. Te thin films were prepared on glass substrate to study the X-ray diffraction. The X-Ray Diffraction and measurement of the electrical properties of the Te films at room temperature with rate of deposition equal to 80 nm/sec for different thicknesses (400-800) nm and different annealing temperatures (373 and 423) K were also studies. The A.C conductivity $\sigma_{a.c}(\omega)$ of Te films with different thicknesses and annealing temperatures has been investigated as a function of frequency and temperatures. The type of charge carriers, carrier concentration (n_H) and Hall mobility (μ_H) have been estimated from Hall measurements. The current –voltage and capacitance–voltage measurements in the dark as well as illumination was done for Te thin films. We can observe that the depletion layer width (W) increases with increasing of the annealing temperature which is due to the decreasing in the carrier concentration which leads to a decrease of the capacitance. The variation of built-in potential (V_{bi}) may be due to the improvement in the structure of the film. The ideality factor and tunneling constant for Te/Si Heterojunction were also studies as a function of thickness and annealing temperatures.

Keywords: Tellurium, Thin films, Electrical properties, X-ray diffraction.

1. Introduction

Te thin films have been extensively used in various technological areas, especially in microelectronic devices such as gas sensor [1−3], optical information storage [4] and other applications [5−7]. All these applications are due to remarkable physical properties of Te such as low band-gap and transparency in the infrared region.

Heterojunction devices of the metal-semiconductor, semiconductor-semiconductor and amorphous semiconductor-crystalline semiconductor types have gained considerable interest from researchers both from a fundamental physics(Such studies include band structure, current transport mechanism and as tools in the analysis of other physical parameters) and technological viewpoint. For example, Chandra and Prasad [8] found that metal-semiconductor contacts (or Schottky barriers) can be used as low temperature sensors. Study of Mimura and Hatanaka [9] (1987) showed that hydrogenated amorphous silicon crystalline silicon heterojunction has application to imaging devices. Kentaro and Nakazawa [10], Lovejoy [11] have also stated that amorphous and polycrystalline thin film semiconductors have possible application in optoelectronics. Cross [12] Xiao and Whitefield [13] have indicated that solar cells based on silicon (Si) and Gallium Arsenide (GaAs) semiconductors can provide power for satellites and water pumping systems.

The experimental data on the electrical and optical properties of Te films showed an important dependence of these properties both on the thickness and the preparation conditions of the films [14-17]. This indicates a strongly correlation between the properties and structure of the film.

The purpose of this study is to measure the electrical properties of thermally evaporated tellurium films on n-type crystalline silicon substrates and assess the junctions for possible device application.

2. Experimental

Te thin films were prepared by thermal evaporation technique in vacuum system supplied by Blazers Model [BL 510] ($\approx 10^{-5}$ Torr) of polycrystalline tellurium powder (99.99% purity). Thin films of Te deposited on glass substrate and on Si wafers for preparation heterojunction Te/ Si. A molybdenum boat of 2895k melting point was used to evaporate Te. It has rectangular solid shape with appropriate depth to prevent material sputtering during evaporation process. Suitable masks were made from aluminum foil, and then cleaned by distilled water and alcohol. An electric current was passed through the boat gradually to prevent breaking the boat, when the boat temperature reached the required temperature the deposition process starts with constant deposition rate. After these steps the current supply was switched off and the samples were left in the high vacuum, and then the air was admitted to the chamber. The films were taken out from the coating unit and kept in the vacuum desiccators until the measurements were made. All the samples were prepared under constant conditions (pressure, substrate temperature and rate of deposition 80nm/s); the main parameters that control the nature of the film properties are thickness (400-800) nm and annealing temperature (373and 423) K. The film thicknesses measured with an interference microscope. The film structures were investigated by standard X-ray diffraction (XRD) technique, using Cu-K_α radiation. The carrier concentrations for the studied films were obtained by using the standard dc techniques for Hall coefficient measurements. The Hall Effect is used to measure certain properties of semiconductors: namely, the carrier concentration (even down to a low level of 10^{12} cm $^{-3}$), the mobility, the type (n or p) and resistivity. For ac- measurement, an HP-R2C unit model (4275 A) multi frequency LCR meter has been used to measure the capacitance (C) and resistance (R) with frequency range between 120Hz-10 kHz, with an accuracy of 0.1%. Ac instrument is shielded by the copper sheet to avoid the distortion signal, and to prohibit the connectors among the experimental portion from becoming a source of noise by using coaxial cables and BNC connectors were used. The current –voltage measurements in the dark as well as illumination was done for Te thin films using Keithly type 616 digital electrometer and d.c power supply. The capacitance–voltage measurements for Tellurium thin films were measured using multi-frequency LCR meter model hp. 4274 A and 4275 A; Hewlett, Packard.

3. Results and discussion

3.1. X-Ray Diffraction for Te Films

The XRD results for Te films prepared at room temperature for different thicknesses (400,500and600) nm are shown in Fig.1. Peaks at 2θ equal to 23.5 and 41, which correspond to (100) and (110) planes shown for films deposited at thickness 400 nm. At thickness 500 nm another peaks at 2θ equal to 28 and 47.5 which correspond to (011) and (200) planes are absorbed. For films deposited at thickness 600nm exhibited another peak at 2θ equal to 50 which correspond to (021) planes. According to JCPDS Data Base, Card No. 96-101-1099 [18], these reflections represent a hexagonal structure. This is agreement with Rusu [19].

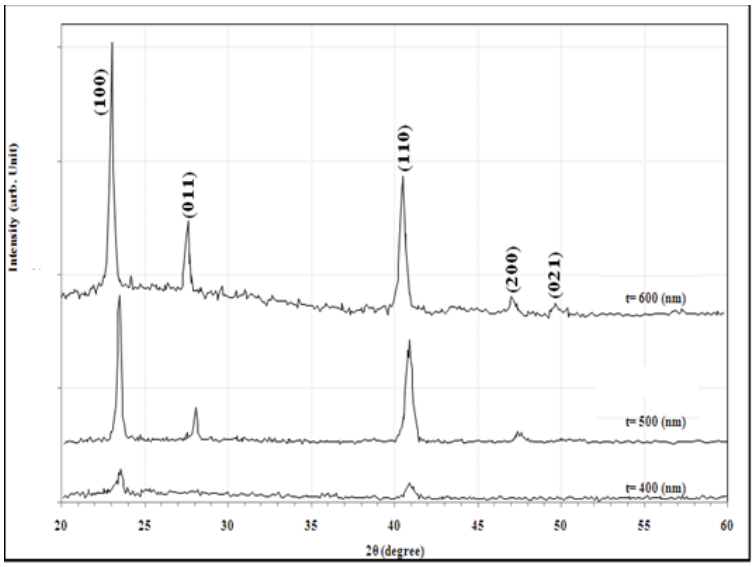


Figure1: X-ray diffraction for Te at thickness 400nm, 500nm and 600nm

Table 1 show the experimental data compared with the standard data.it was found that the values of grain sizes varied from 197.9to 272.2A^{o} for films of thickness 400-600nm respectively at plane (100).This result agree with Balasubramaniam [20].

Table (1) X-ray diffraction data for Te

t (nm)	2theta Exp. (degree)	d Exp. (Å)	I/I_0 Exp. %	d std. (Å)	I/I_0 std. %	hkl	Grain Size (Å)
400	23.549	3.775	100	3.857	11	(100)	197.9
	40.975	3.201	55	2.227	25	(110)	145.4
500	23.521	3.779	100	3.857	11	(100)	271.4
	28.065	3.177	21	3.232	100	(011)	342.6
	40.887	2.205	65	2.227	25	(110)	179.2
	47.601	1.909	10	1.928	2	(200)	173.7
600	23.075	3.851	100	3.857	11	(100)	272.2
	27.561	3.234	28	3.232	100	(011)	267.5
	40.508	2.225	52	2.227	25	(110)	208.1
	47.01	1.931	10	1.928	2	(200)	206.3
	49.66	1.834	8	1.834	17	(021)	203.6

For the as deposited Te films at thickness 600 nm and annealing to temperatures (373 and 423)K (as shown in fig.2), the XRD pattern displays strong reflections at (100) and (110) direction as well as the low intensity peaks at (011), (111) and (200) for film annealed to 373K and (011), (012), (200) and (021) for film annealed to 423K with hexagonal structure. From this figure we can see that the intensity of (100) plane increase and become sharp as the annealing temperature increase. Our results agree with Rusu [19] and Ott and Gunter [17].

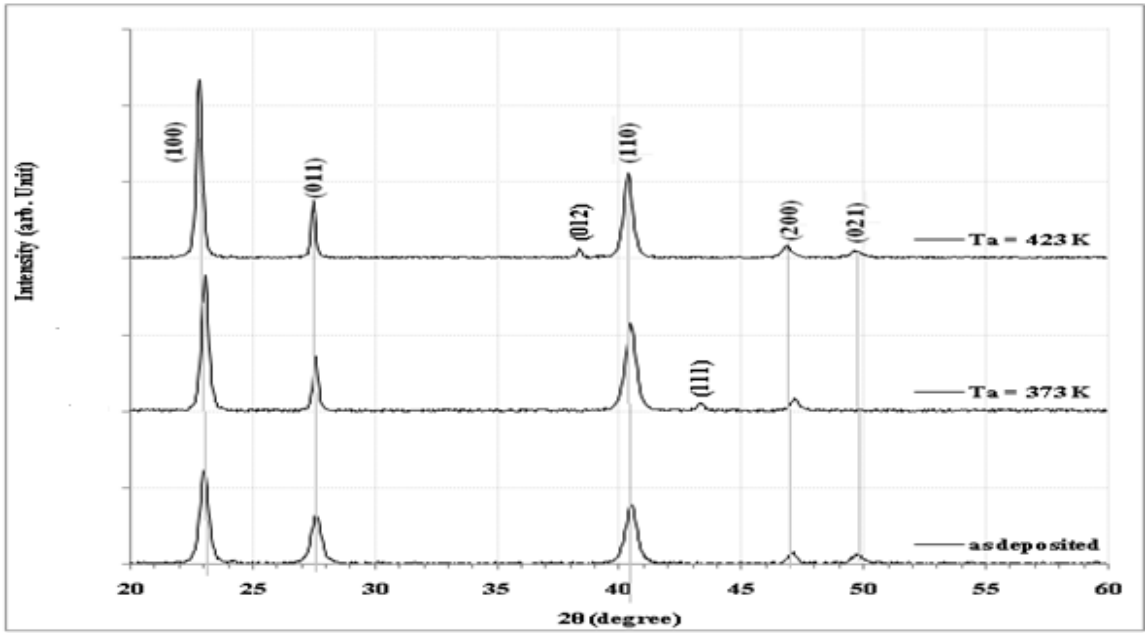


Figure 2: X-ray diffraction for Te at t=600nm a) as deposited b) annealed to 373 K c) annealed to 423 K

Table 2 show the experimental data (FWHM, d_{hkl} and the grain size) at different annealing temperatures compared with the standard data. We can see the grain size increase with increasing of annealing temperature and increase with increasing of thickness.

Table (2) X-ray diffraction data for Te thin films at thickness 600nm as a function of annealing temperatures.

T_a (K)	2ɵ (degree)	Fwhm (degree)	Int (arb unit)	d_{hkl}Exp. (Å)	G.S (Å)	d_{hkl} Std. (Å)	hkl
As deposited	22.994	0.395	618.1	3.865	193.10	3.857	(100)
	27.571	0.452	321.6	3.233	170.48	3.232	(011)
	40.452	0.508	392	2.228	156.84	2.227	(110)
	47.062	0.395	70.4	1.929	206.38	1.928	(200)
	49.718	0.508	60.3	1.832	162.19	1.833	(021)
373	23.022	0.323	891.6	3.860	236.64	3.857	(100)
	27.543	0.242	355.2	3.236	318.37	3.232	(011)
	40.433	0.484	566.4	2.229	164.70	2.227	(110)
	43.298	0.323	46.7	2.088	249.58	2.084	(111)
	47.135	0.403	74.8	1.927	202.35	1.928	(200)
423	22.788	0.262	1167.7	3.899	290.86	3.857	(100)
	27.460	0.202	366.5	3.245	381.46	3.232	(011)
	38.349	0.163	68.3	2.345	487.22	2.349	(012)
	40.334	0.403	550.3	2.234	197.86	2.227	(110)
	46.820	0.403	75.8	1.939	202.14	1.928	(200)
	49.661	0.505	42.2	1.834	163.19	1.833	(021)

3.2. Hall measurements

The type of charge carriers, carrier concentration (n_H) and Hall mobility (μ_H) have been estimated from Hall measurements. The variation of Hall voltage with the current for Te films deposited at R.T for different thicknesses and annealing temperatures have a positive Hall coefficient (p-type charge carries).

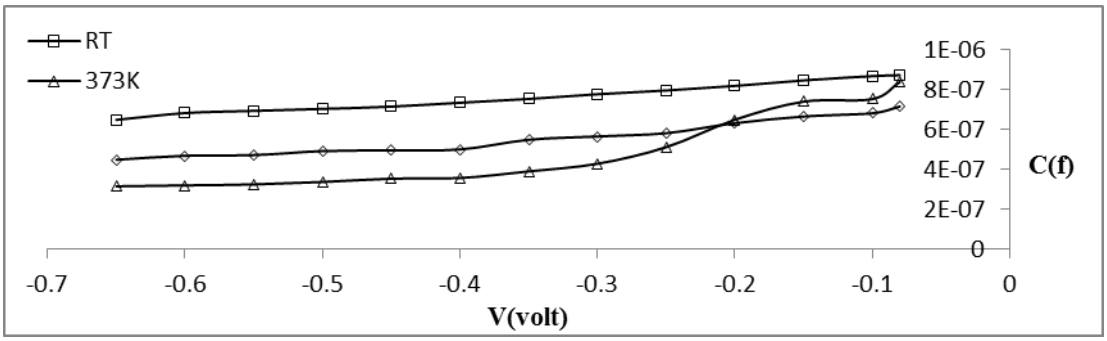
Table 3 shows the variation of carrier's concentration and Hall mobility with thickness at different annealing temperatures of Te films. It can be observed from the table that both the carrier's concentration and mobility increase with increasing of annealing temperatures while the mobility increase with increasing of thickness but carrier's concentration decrease with increasing of thickness. These results agree with Dutton and Muller [21], Rusu [19], and with Capers and White [22].

Table 3: Hall parameters for Te films at different thicknesses & annealing temperatures.

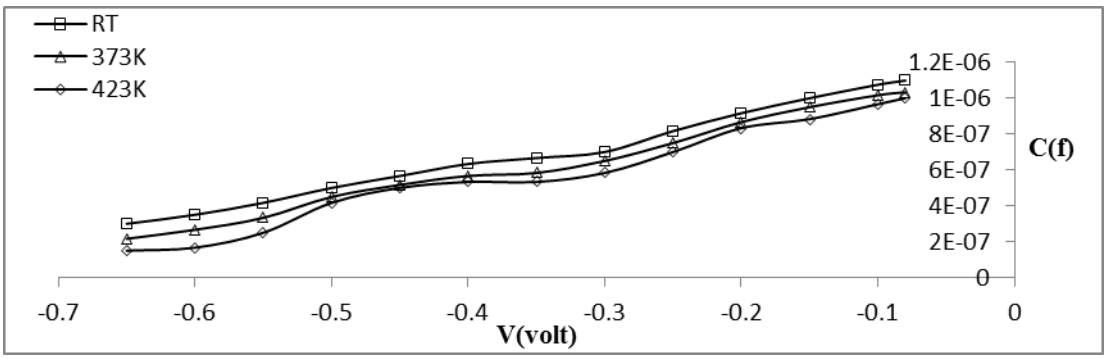
Thickness (nm)	T_a (K)	n_H	μ_H
		$\times 10^{18}$ (cm^{-3})	($cm^2/V.s$)
400	R.T	7.76	5.17
	373	8.01	7.2
	423	9.83	8
500	R.T	7.64	6.2
	373	7.90	9.2
	423	9.40	10
600	R.T	5.97	7.15
	373	7.04	10
	423	9.14	11.9
700	R.T	4.91	14
	373	6.84	17.7
	423	7.80	18.2

3.3. C-V Characteristic of Te/Si Heterojunction

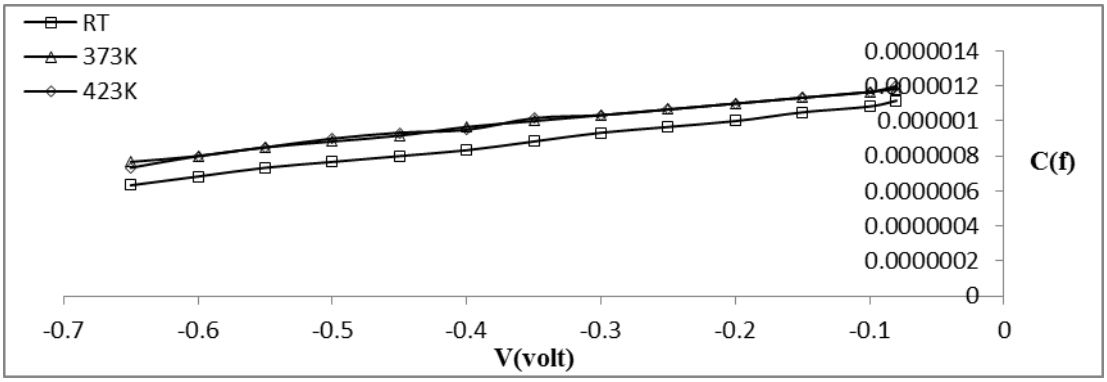
Figure (3a, b and c) shows the junction capacitance variations as a function of the reverse bias (0 – 0.7) volt at frequency equal to 100Hz for Te/Si heterojunction for different annealing temperatures at thicknesses 400nm, 600nm and 800nm respectively.



(a)



(b)

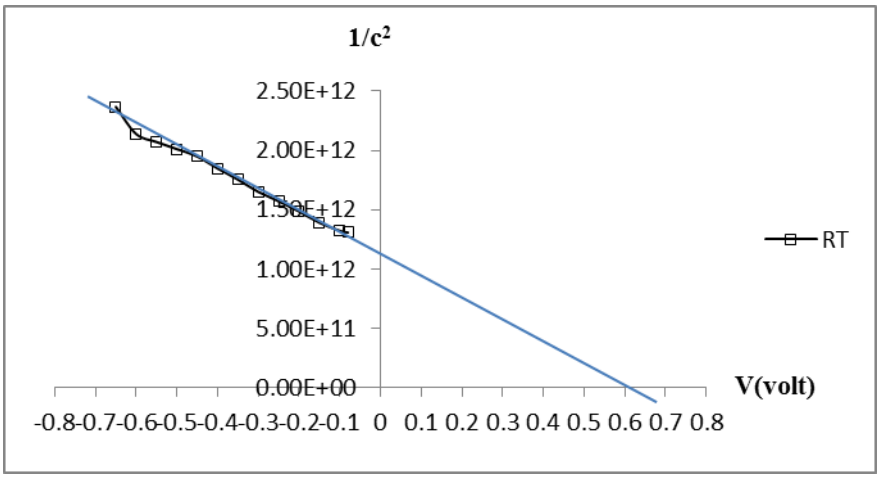


(c)

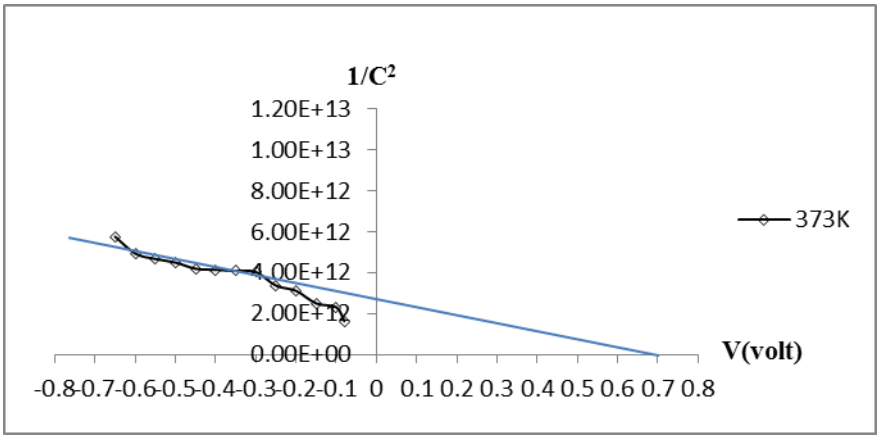
Figure 3: The variations of capacitance versus reverse bias voltage for Te/Si heterojunction for different annealing temperatures at thickness (a): 400nm, (b): 600nm (c): 800nm.

It is clear that the capacitance decreases with increasing of the reverse bias voltage and annealing temperature. Such behavior is attributed to the increasing in the depletion region width, which leads to increase the value of built-in potential.

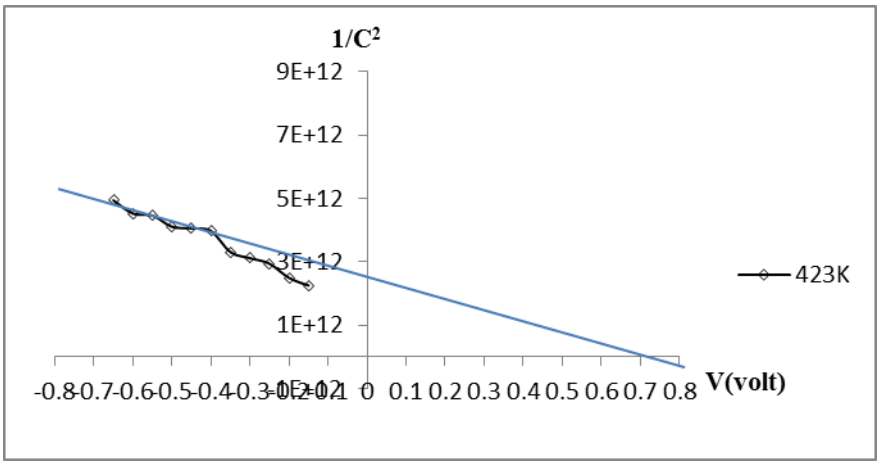
The inverse capacitance square is plotted against applied reverse bias voltage for Te / Si heterojunction at different annealing temperatures for thickness 400nm, 600nm and 800nm and shown in Figures 4, 5 and 6 respectively. The plots revealed straight line relationship which means that the junction was of p- type.



(a)

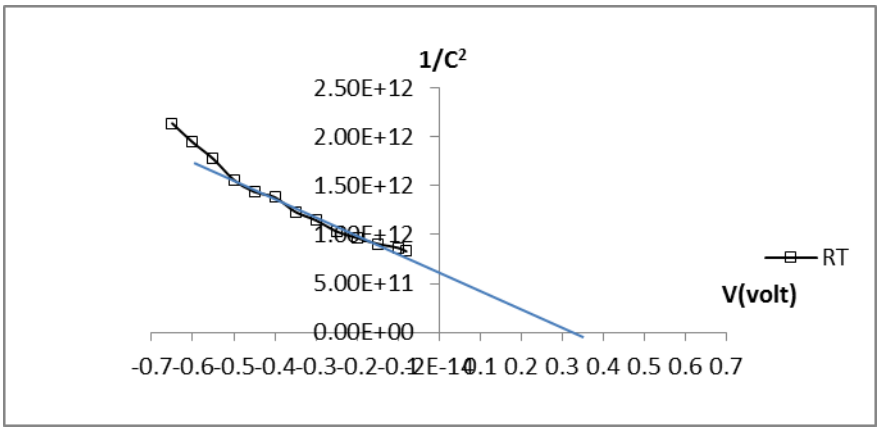


(b)

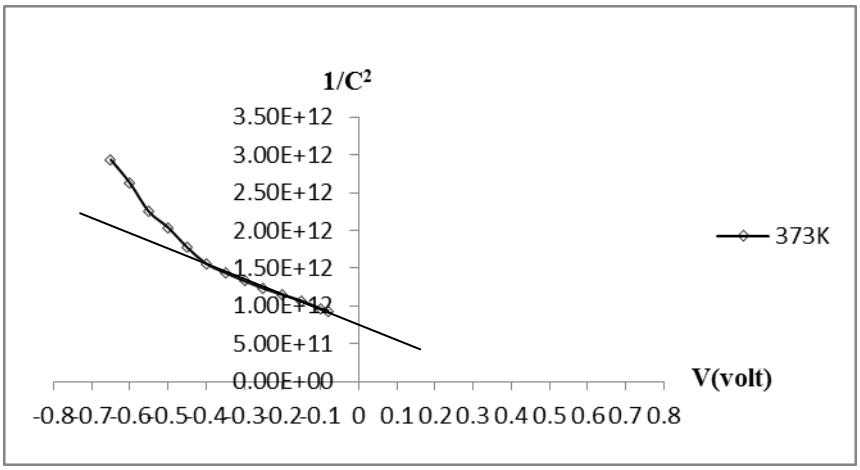


(c)

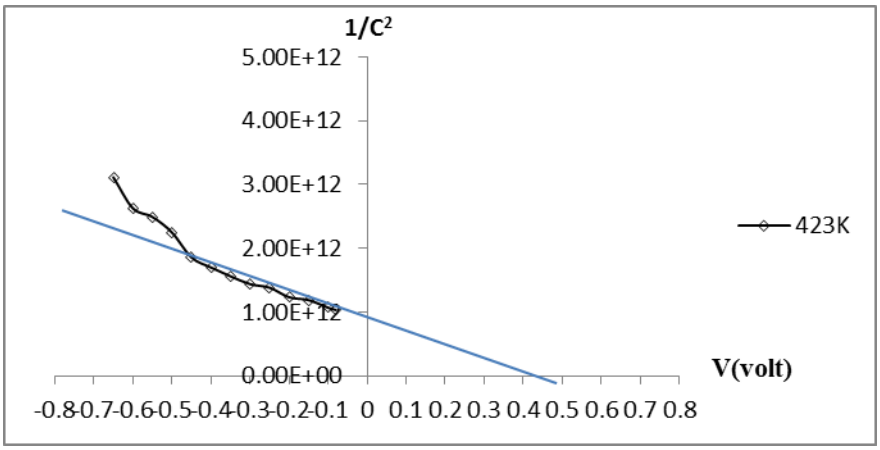
Figure 4: The variation of $1/C^2$ versus reverse bias voltage for Te/Si heterojunction for thickness 400nm at different annealing temperatures a): RT (b): T_a=373k and (c): T_a=423k.



(a)

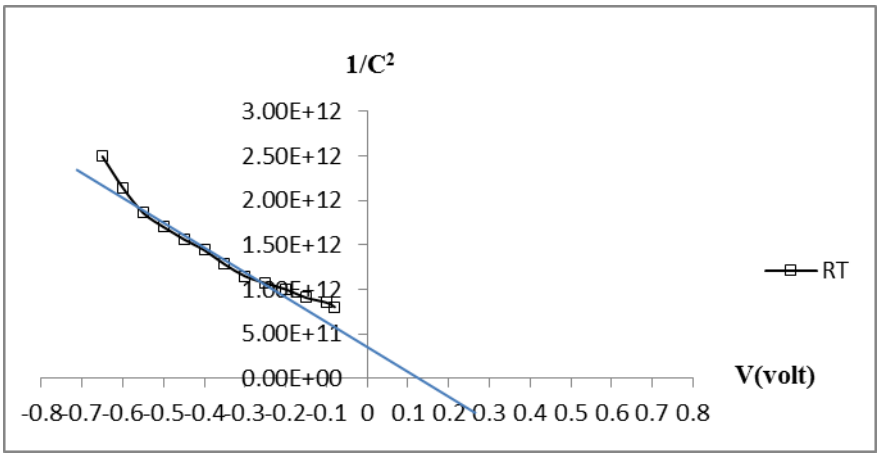


(b)

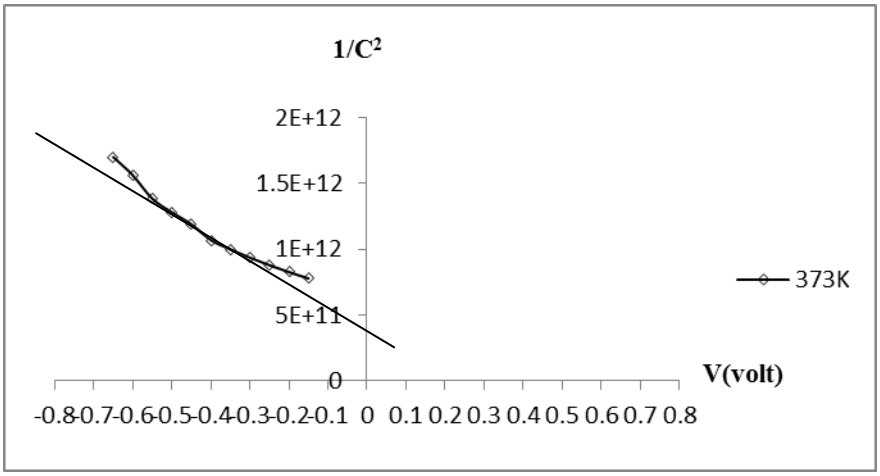


(c)

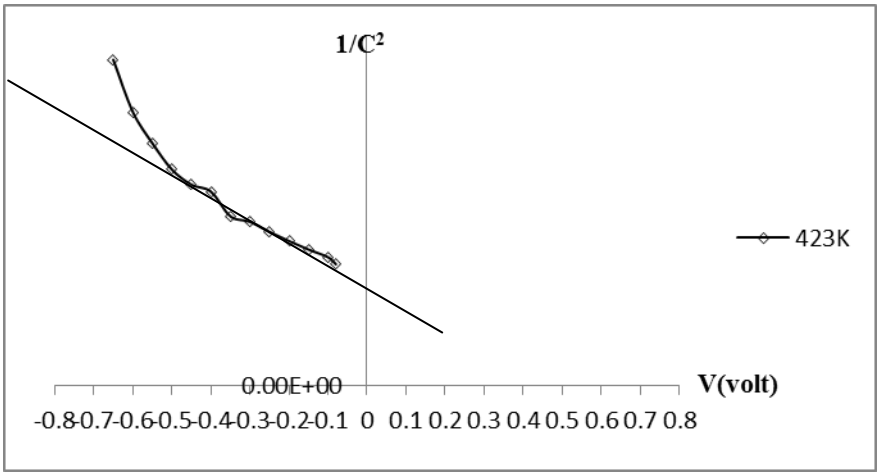
Figure 5: The variation of $1/C^2$ versus reverse bias voltage for Te/Si heterojunction for thickness 600nm at different annealing temperatures (a): RT, (b): T_a=373k and (c): T_a=423k.



(a)



(b)



(c)

Figure 6: The variation of $1/C^2$ versus reverse bias voltage for Te/Si heterojunction for thickness 800nm at annealing temperatures (a): RT, (b): T_a=373k and (c): T_a=423k.

The interception of the straight line with the voltage axis at ($1/C^2 = 0$), represents the built-in potential and the carrier's concentration corresponding to the slope of the $1/C^2$ vs. applied Voltage.

We can observe from Table (4), that the capacitance at zero bias voltage (C_o) decreases with the increasing of the annealing temperatures for Te/Si junctions and this behavior is due to the surface states which leads to an increase in the depletion layer and a decrease of the capacitance. We can observer that the depletion layer width W increases with increasing of the annealing temperature which is due to the decreasing in the carrier concentration which leads to a decrease of the capacitance. The variation of built-in potential (V_{bi}) may be due to the improvement in the structure of the film. This result is coincident with Iyayi and Oberafo [23].

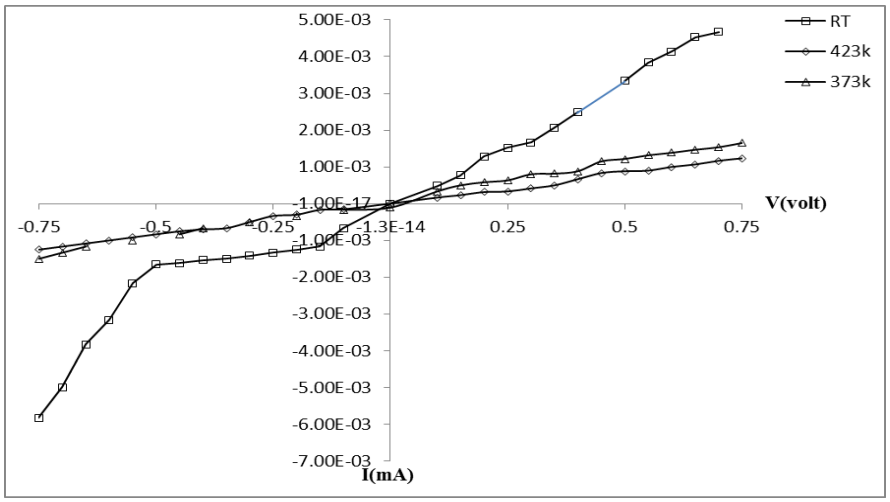
Table 4: Values of $C_{o,}$ W and V_{bi} for Te/Si heterojunction with different thicknesses and annealing temperatures.

Thickness (nm)	T_a (K)	C_o (F) $X10^{-6}$	W (μm) $X10^{-6}$	V_{bi} (Volt)
400	R.T	0.9	758471.2	0.61
	373	0.73	935101.5	0.66
	423	0.71	975177.3	0.7
600	R.T	1.38	494655.2	0.32
	373	1.35	505647.5	0.35
	423	1.20	568853.4	0.4
800	R.T	1.42	480721.2	0.13
	373	1.4	487588.7	0.23
	423	1.15	595138.7	0.45

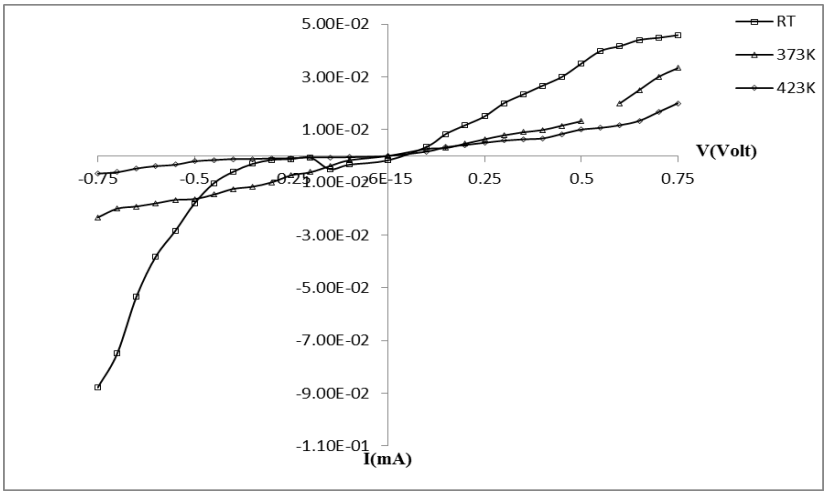
3.4.I-V Characteristics for Te/Si Heterojunction under Dark:

One of the important parameters of a heterojunction measurement is a current-voltage characteristic which explains the behavior of the resultant current with the applied forward and reverse bias voltage. Figure 7 shows I-V characteristic for Te/Si heterojunction at forward and reverse bias voltage for different annealing temperatures for thickness 400nm, 600nm and 800nm.

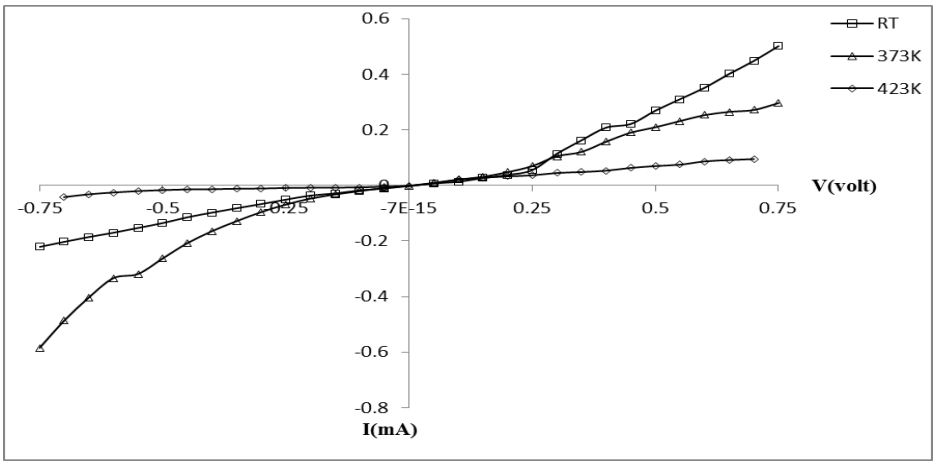
There are two regions for the forward current curves, the first region for the voltage range (0-0.3Volt) which the recombination current is dominate and the second region (V>0.3 volt), the variation is of exponential type and it is due to the tunneling current [24]. An analysis of the forward- and reverse biased current-voltage characteristics of the junctions show rectification properties. For forward voltages, V_F <1.0V, the forward characteristics shows exponential behavior, the current increasing rapidly with voltage according to equation $I_F \sim \exp(qV_F/ßK_BT)$ [where K_B is the Botzman's constant, q is the electronic charge, T is the absolute temperature and (ß) is the ideality factor defined as $[(q/ K_BT)\partial V_F / \partial(\ln I_F)]$. As the bias is increased further, deviation from this exponential behavior sets in with the current increasing less and less rapidly than $\exp (qV_F/ ß K_BT)$. Kuech [25] attributes such a drop in exponential rate of increase of forward current with increasing bias to the influence of an appreciable series resistance on the junction characteristics [26]. So from the logarithm of the initial part of the forward current, the ideality factor (ß) could be calculated. From the second region in Figure 7 the tunneling constant (A_t) can be calculated. The ideality factor decreases with the decreasing of annealing temperature as shown in Table (5). The ideality factor (ß) *is* unity when the current flow across the diode is controlled by thermoionic emission, and it increases with the degradation of the diode characteristics or with other superimposing transport mechanism [27]. It should be noticed here that the ß gives indication about the defects in heterojunction, a high value indicates structural defects [28]. Tellurium has a large density of states at the Fermi level, which reveals the more "metallic" behavior in this material. These large densities of states make it reasonable that they contribute more significantly to the electrical conduction in c-Te/n-Si.



(a)



(b)



(c)

Figure 7: I-V characteristics in the dark for Te/Si heterojunction at different annealing temperatures at thicknesses (a):400nm, (b): 600nm and (c): 800nm.

Further analysis of the current-voltage characteristics of the junctions show that the room electrical conductivity is decreased after post-deposition heat treatment (annealing). As shown in figure 7, the current densities of the annealed junctions are lower than that for the as-deposited (un-annealed) junctions. The localized states at the interface of the junction and the high density of localized states in the bulk of amorphous layer contribute significantly to the electrical conductivity. In fact, the dominant current mechanism in the amorphous layer of the junction is essentially by hopping between the localized states. However, annealing reduces the number of these states and therefore the conductivity.

Table (5) values of ideality factor and tunneling constant for Te/Si Heterojunction.

Thickness(nm)	T_a(K)	β	A_t
400	RT	2.869	2.483
	373	2.549	2.409
	423	1.684	2.296
600	RT	2.605	2.514
	373	2.790	1.722
	423	1.295	1.541
800	RT	3.749	3.764
	373	3.521	2.577
	423	2.79	3.485

In general, the forward dark current is generated by the flow of minority carriers. The applied voltage injects majority carriers which decreases the built-in potential, as well as the width of the depletion layer. The majority and minority carrier concentration is higher than the intrinsic carrier concentration ($n_i^2<n_p$) which generate the recombination current at the low voltage region (0-0.3 Volt). This is because the excitation of electrons from valence band to conduction band will recombine them with holes that are found at the (V.B). This is observed by the little increase in the recombination current at low voltage region [29], while the tunneling current occurs at the high voltage region (V>0.3 Volt). After that there is a fast increase in the current with increasing the voltage; this is called diffusion current [30].

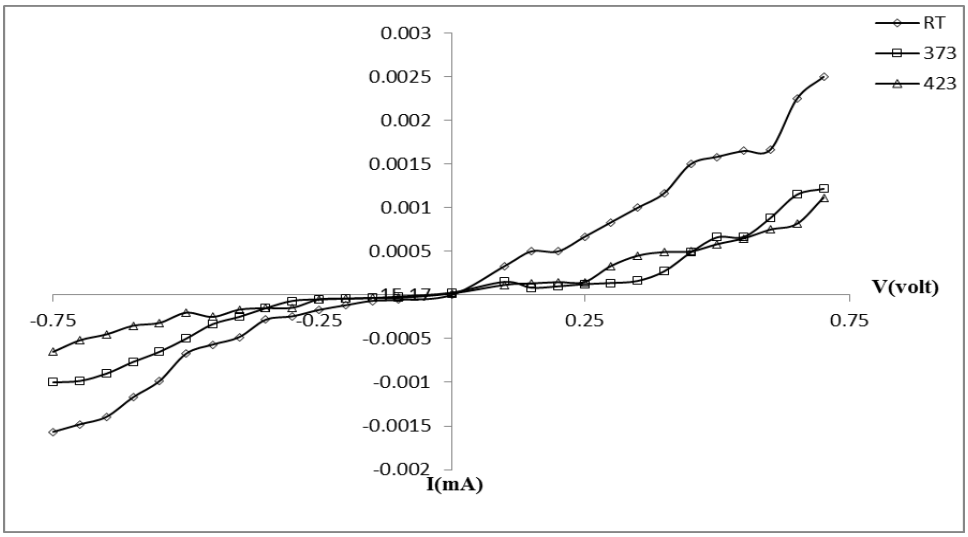
3.5. I-V Characteristic for Te/Si heterojunction under illumination:

The relation between the photocurrent density (J_{ph}) and bias voltage (V) of the Te/Si Heterojunction at different thicknesses and annealing temperatures are presented in Fig. (8 a, b and c). The measurements were carried out under power density 60 mW/cm^2. From these figures we observe that the photocurrent density increases with increasing of the bias voltage, i.e. J_{ph} increases with increasing of the depletion region width (W) according to the relation below [31];

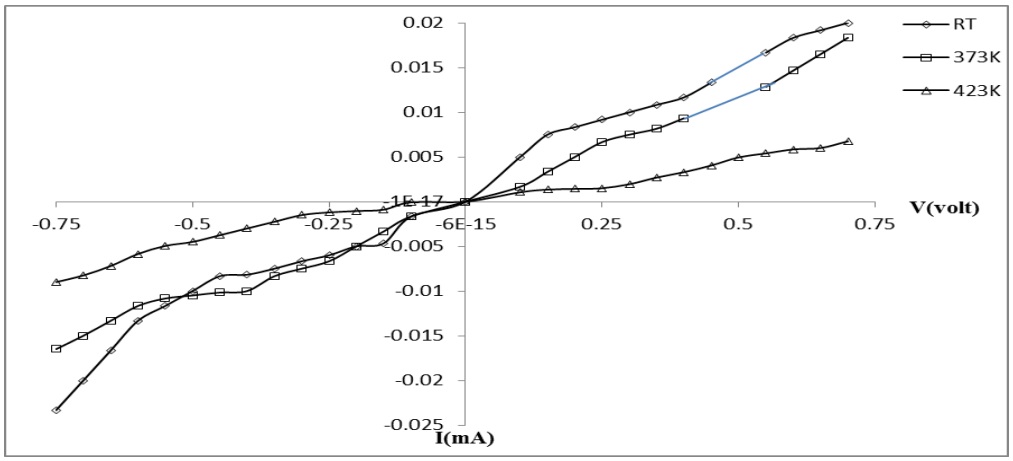
$$I_{ph} = qa\, G_{ph} (L_p + L_n + W)$$

where q is the electron charge, a is the lattice constant, G_{ph} is the generation rate of photo carriers, L_p and L_n are the diffusion length of holes and electrons respectively.

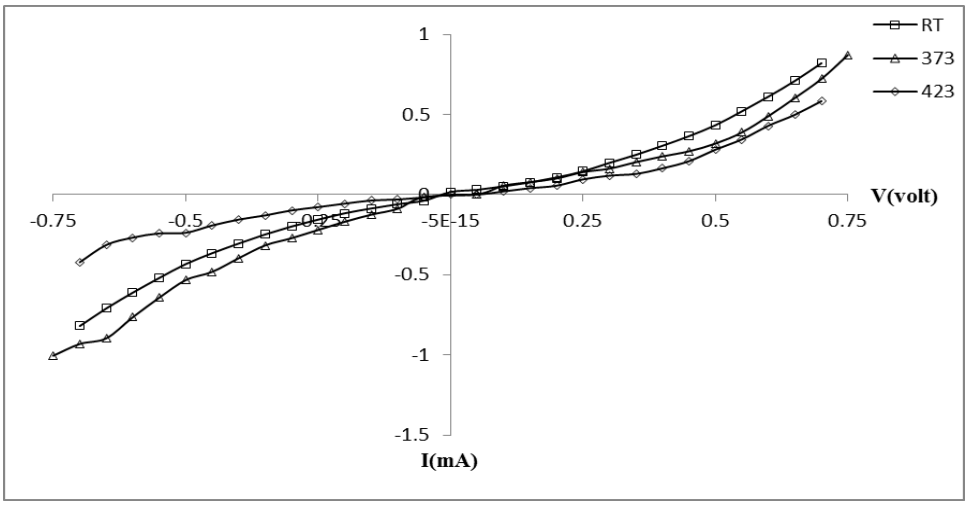
The width of the depletion region increases with increasing the applied reverse bias voltage, which leads to separate the electron-hole pairs and then increase the photocurrent density. The forward and reverse bias photocurrent density is a function of the generation and diffusion carriers. We can also observe from Figure (8a, b and c) that the photocurrent density increases with increasing annealing temperature and films thickness. This is attributed to the increasing in the grain size and reducing the grain boundaries and improvement of structure which leads to the increase of the mobility and increase the photocurrent density as well as the increase of the depletion width which leads to an increase of the creation of electron-hole pairs.



(a)



(b)



(c)

Figure 8: I-V characteristics for Te/Si heterojunction for power density 60 mW/cm^2 at different annealing temperatures at thicknesses (a): 400nm, (b): 600nm, (c): 800 nm.

4. Conclusions

The type of charge carriers, carrier concentration (n_H) and Hall mobility (μ_H) have been estimated from Hall measurements. The depletion layer width increases with increasing of the annealing temperature which is due to the decreasing in the carrier concentration which leads to a decrease of the capacitance. The variation of built-in potential may be due to the improvement in the structure of the film. The ideality factor and tunneling constant for Te/Si Heterojunction were also studies as a function of thickness and annealing temperatures. The room temperature (298K) current voltage characteristics of c-Te/n-Si heterojunctions are studied. The heterojunctions show rectification properties, hence can be used as rectifying devices in electronic appliances. The electrical conductivity in the junctions decreases with annealing.

References

[1] D.Tsiulyanu, S.Marian, H.D.Liess, Effect of annealing and temperature on the NO_2 sensing properties of tellurium based films, Sensors and Actuators B, 2004, 100(3): 380−386.

[2] S.Shashwati, K.P.Muthe, N.Joshi, Room temperature operating ammonia sensor based on tellurium thin films, Sensors and Actuators B, 2004, 98(2−3): 154−159.

[3] D.Tsiulyanu, S.Marian, V.Miron, High sensitive tellurium based NO_2 gas sensor, Sensors and Actuators B, 2001, 73(1): 35−39.

[4] P.Josef, P.Dana, B.Jaroslav, Nano-structured crystalline Te films by laser gas-phase pyrolysis of dimethyl tellurium, Anal Appl. Pyrolysis, 2004, 71(2): 739−746.

[5] L.Lozzi, S.Santucci,S.DI Nardo, XPS, LEED and AFM investigation of the Si(100) surface after the deposition and annealing of tellurium thin films, Surface Science, 1996, 352−354: 1027−1032.

[6] L.Lozzi, S.DI Nardo, M.Passacantando, Growth of Te thin films deposited at room temperature on the Si(100) surface, J of Electron Spectroscopy and Related Phen, 1995, 71(1): 39−45.

[7] L.Lozzi, S.DI Nardo, M.Passacantando, Electron spectroscopy investigation of Te thin films deposited at room temperature on Si(100), Surface Science, 1995, 331−333(1): 569−574.

[8] M.M.Chandra, M. Prasad,(1983), Schotkky barrier characteristics at low temperatures, Phy. Stat.Sol. (a) 77:715-719.

[9] H. Mimura,Y. Hatanaka, (1987), The use of amorphous crystalline silicon heterojunction for the application to imaging device. J. Appl. Phys, 66:2572-2580.

[10] I.Kentaro, T.Nakazawa, (1988), Electrical and optical properties of stannite-type quarternary semiconductors thin films, Japanese Journal of Applied Physics, 27:2094-2097.

[11] D. Lovejoy, (1992). Photovoltaics for rural electrification, In: Sayigh A.A. (ed). Renewable Energy-Technology and Environment, Exeter,Pergamon Press, Vol. 1:124-132.

[12] Cross, T.A. (1992), Photovoltaics for commercial space applications: The move to Gallium Arsenide solar cells. In: Sayigh A.A. (ed). Renewable Energy – Technology and the Environment. Exeter, Pergamon Press Vol. 1.p212-221.

[13] L.J Xiao, G.R. Whitefield, (1992), A solar photovoltaic water pumping system for Chinese villages. In:Sayigh A.A. (ed), Renewable Energy-Technology and the Environment. Exeter. Pergamon Press, Vol. 1:323-327.

[14] I. Yamamoto, Y. Ohmasa, H. Ikeda, H. Endo, The optical properties of tellurium under high pressure, J. Phys.: Condens. Matter. 7, 4299 (1995).

[15] H. Akbarzadeh and M.R. Mohammadizadeh, The influence of generalized gradient corrections on the structural and electronic properties of tellurium, computational material science, vol.8, No.4, 335-340, 1997.

[16] M. Rusu, On thickness dependence of electrical and optical properties of Te thin films, Applied Physics A: Materials Science & Processing,Volume 66, Number 3, 357-361,1998

[17] P. Ott, J. R. Gunter, Electron microscopic study of the epitaxial growth of thin single crystalline tellurium films on NaCl (001),Thin Solid Films, 366(1-2), 100 (2000).

[18] JCBDS Data Base,Card No.96-101-1099.

[19] M.Rusu,on the electrical and optical properties of the stratified Tellurium thin films,J.of electronics and Advanced Materials, vol 3,No.4,2001,867-872.

[20] T.Balasubramaniam, Saknarayandass and D. Mangalara,electrical properties of thermally evaporated Tellurium thin films Bull.mat.sci,vol.30,No.1,1997,p.79-92.

[21] W.R.Dutton,R.S.Muller, Electrical Properties of Tellurium Thin Films,Proceeding of The IEEE,vol.59,No.10,Oct. 1971,p.1511.

[22] M. J. Capers, M. White, The electrical properties of vacuum deposited Tellurium films, Thin solid films, 15(1973), p.5-14.

[23] S.E.Iyayi and A.A.Oberafo, Studies on a-Se/n-Si and a-Te/n-Si Heterojunctions, Journal of Applied Sciences & Environmental Management, Vol. 9, No. 1, 2005, pp. 143-145

[24] S.R.Elliot,Adv. phys. 36 (1987) 135-218.

[25] T.F. Kuech, C.S.Wu, S.S. Lau, (1984). The measurement of silicide Schottky barrier heights by use of photovoltage techniques. Mat. Res.Soc. Symp. Proc., 25: 663-665.

[26] T.Okumaru, K.N. Tu, (1987). Electrical characterization of Schottky contacts of Au, Al,Gd and Pt on n-type and p-type GaAs. J. Appl.Phys., 61:2955-2961].
[27] K. Skimakawa, Phil. Mag. B 46 (1982) 123.
[28] A. M. Phahle, on the electrical properties of thermally evaporated tellurium films, J. of thin solid films,vol 41,1977, p.235-241.
[29] Y. Gaing, R. Hong, Adv. Mat. 15 (2003)1195.
[30] S. Goto and Y. Nomura, J. Appl. Phys. 34 (1995) 1180.
[31] Y. Murchta and Z. Hirol, J.Appl.Phys.Lett.85 (2004) 2950.