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Efficient Quantum-Dot Cellular Automata for Half Adder using Building Block

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Abstract: Quantum-dot cellular automata (QCA) are nanoscale digital logic devices that use electrons in arrays of quantum dots to perform binary operations. In this paper, an efficient quantum-dot cellular automata for half adder circuit will be proposed using the basic building blocks where the configuration cells have been customized to implement the half adder circuit. It will be shown that the proposed design has less cell count and/or better latency better than proposed designs in the literature.

Keywords: Quantum-dot Cellular Automata, Logic Circuit, Half Adder, Building Block

1 Introduction

A quantum-dot cellular automaton (QCA) is a promising emerging technology that works on novel paradigms such as synthesis of reversible gates [1,2]. QCA is a constructing nanoelectronic technology that gives another approach to computation at nano level [3]. Research and development in the field of electronic devices during the last decades made it possible for designers to increase the speed and decrease the size of the components and the power consumption. QCA is based upon the encoding of binary information in the electron charge configuration within quantum dot cells. Computational power is provided by the Coulombic interaction between QCA cells. There is no current flow between cells and no outer source is delivered to singular internal cells [4]. Due to the reordering of electron positions, the physics of cell-to-cell interaction provides the local interconnections between cells [5,6]. Tougaw and Lent in 1993 introduced the basic concepts of QCA [3,7] as the computation with cellular automata consists of arrays of quantum-dot cells. The unique feature is that logic states are represented by a cell. A cell is a nanoscale device able to encode data by two-electron configuration. The cells must be aligned exactly at nanoscale to provide correct functionality, thus, the testing of these devices for misalignment and manufacturing errors has an important role for the correctness of circuits [8]. The relation between computation and data loss has been solved in QCA because it has very low power consumption which is a common property for QCA [9,18,19]. In [10,12], different QCA designs for half adder circuit have been shown.

Many designs for the half adder circuit using QCA have been proposed. In 2011, S. Karthigai Lakshmi and G. Athisha [11] proposed a design of half adder. The proposed design consists of 77 cells. It uses three MV gates, one MV gate is used as OR gate, while the second and third MV gates are used as AND gate. The proposed design has 1 clock delay. In 2014, Subhashee et.al. [12] proposed a design of half adder circuit which consists of 80 cells. It uses three MV gates, one MV gate is used as OR gate, while the second and third MV gates are used as AND gate. The proposed designs have 1 clock delay. In 2014, Santra S and Roy U [10] proposed a design of half adder circuit which consists of 64 cells. It uses four MV gates, one MV gate is used as OR gate, while the second, third, and the fourth MV gates are used as AND gate. The proposed design has 1 clock delay and it is better than the other designs in terms of cell count but it uses four MV gates while the others use three MV gate only.

The aim of this paper is to propose QCA design for half adder circuits that contain more than one logic gate such as half adder. The proposed QCA circuits in this paper have been designed and simulated using the

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QCADesigner tool version 2.0.3 running the system with coherence simulation engine [13].

This paper is organized as follows. A review of the QCA basics and clocking are given in Section 2. The proposed QCA for the half adder circuit is shown in Section 3. Finally Section 4 concludes the paper.

2 QCA Basics

Before addressing the proposed layouts, it is important to review the basic properties of QCA. This section gives a brief overview of the device physics, basic logic gates, and clocking.

2.1 Basic Quantum Dot Construction

The computational elements and wires of an entire circuit are built through QCA devices. The basic component of a QCA device is a cell with four quantum dots placed in the corners and two free electrons. By applying sufficient local electric field on the tunneling junctions, the potential barriers control the transition of the mobile electrons to provide three states for the isolated cell. The first state is null cell occurs when the barriers are lowered by decreasing the electric field, this allows electrons to be found on any dots. The second state is positive polarization (p=+1) occurs when the barriers are raised positively. The third state is negative polarization (p=-1) occurs when the barriers are raised negatively. The terms positive polarization and negative polarization are corresponding to binary logic values 1 and 0 respectively. Figure 1. shows the basic QCA cells and their possible polarizations. Coulombic interactions between the cells placed near each other to be forced into matching polarizations. More details for the QCA device physics can be found in [3].

Fig. 1: QCA cell polarization

2.2 QCA Wires

In a QCA wire, the binary information move from input to output because of the Coulombic interactions between cells. The propagation in a 90 QCA wire is shown in Figure 2a. A 45 QCA wire, as shown in Figure 2b, is also possible where the propagation of the binary signal alternates between the two different polarizations +1 and -1 [14].

2.3 QCA Majority Gate and Inverter

The main QCA logical circuit is the three-input MV gate as shown in Figure 2c. The MV gate consists of five QCA cells, three input cells, one device cell and one output cell [13]. Suppose that the three inputs are a, b and c, then the logic function of the MV gate is $M(\mathrm{a,b,c}) = ab + bc + ac$, where $a + b$ denotes a OR b, and ab denotes a AND b. By using the MV gate, we can construct the OR and the AND gates by fixing the polarization of one of the inputs of the MV gate to P = +1 (logic 1) and P = -1 (logic 0) as shown in Figure 3. Another popular QCA gate is the NOT gate or the inverter. One construction of QCA inverter is shown in Figure 4a. Other construction of the NOT gate is shown in Figure 4b, where the input is inverted due to the different polarization that are misaligned between the touching corners of the cells [17]. The NAND gate can be constructed using the AND gate followed by the NOT gate as shown in Figure 5.

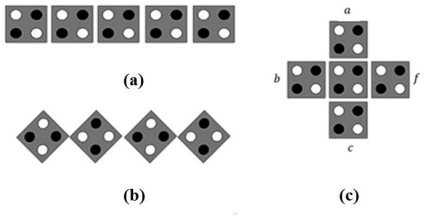

Fig. 2: (a) QCA wire (90), (b) QCA wire (45), (c) QCA majority gate

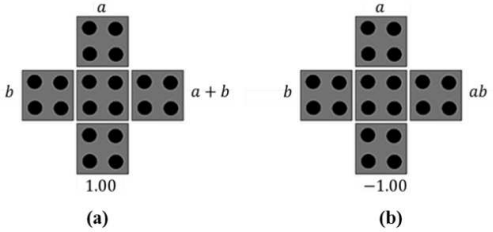

Fig. 3: QCA layout of: (a) OR gate, (b) AND gate

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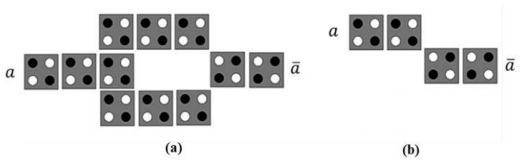

Fig. 4: QCA inverters

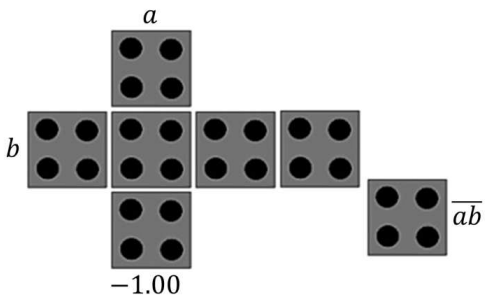

Fig. 5: QCA layout of NAND gate

2.4 QCA Clocking

Synchronization and control of information flow are provided by QCA clocking to give the power to run the QCA circuit because there is no outer source for that purpose. All the proposed designs in this paper have been simulated using coherence simulation engine with clock high = 9.8e- 22 J and clock low = 3.8e-23 J [14]. The QCA clocking is achieved by managing the potential barriers between adjacent quantum-dots. Controlling the potential barrier by raising or lowering allows full control of localization and polarization for the mobile electrons as following: raising potential force elements to localize and hence definite polarization occur while the lowering potential allows delocalizing electrons and providing no definite cell polarization. The cells can be grouped into four zones to have the same electric field influence to achieve proper clocking scheme. These four zones are as follows: switch zone occurs when the tunneling barriers are raised causing the electrons to be effected by Columbic charges of neighboring zones. The hold zone has high tunneling barrier and will not change the state but influence adjacent zones. The release and relax zones occur by decreasing the tunneling barrier, so, other zones will not get influenced by that zone as shown in Figure 6. It is important to note that the size of these zones must be within certain limits, but their shape may be irregular [16]. The accurate placement of these zones is important for the efficiency of the design.

3 QCA for Half Adder

The half adder circuit has two inputs variables x and y and two outputs variables sum and carry. The half adder circuit has the following logic operation: sum=x⊕y and carry=xy. The truth table of the half adder circuit is shown in Table 1.

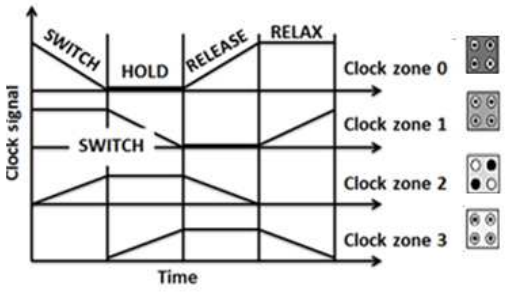

Fig. 6: The four phases of the QCA clocking

The basic building block proposed in [15] consists of two MV gates and NOT gate. One of the MV gates functions as AND gate, while the other functions as OR gate. The basic building block contains 27 cells, 11 of them will function as configuration cells and will be denoted as $x_1, x_2, \ldots, x_{11}$, where these configuration cells will be set as input cells, output cells, device cells, rotate cells or control cells as shown in Figure 7.

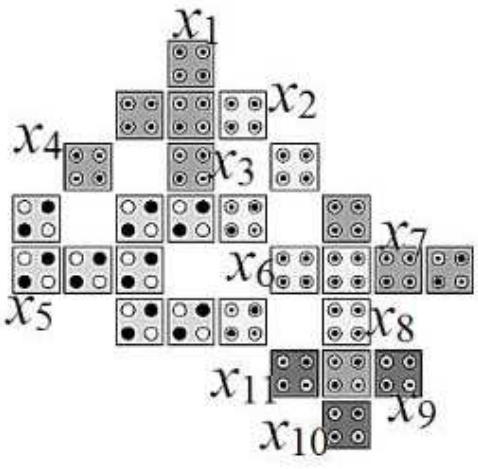

Fig. 7: The basic building block where the customization cells are $x_1, x_2, \ldots, x_{11}$ [15]

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Table 2: Customization of the 11 configuration cells $x_1, x_2, , x_{11}$ of the proposed basic building block where DC denotes device cell, OC denotes output cell, IC denotes input cell, and RC denotes rotate cell.

Configuration cells	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	x_{10}	x_{11}	Number of added cells
Half adder circuit in Table 1	-1.0	DC	1.0	-1.0	IC	DC	DC	DC	1.0	1.0	1.0	21

Table 1: The truth table of the half adder circuit

Input		Output	
x	y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The basic building block can be customized to implement half adder by adding 21 cells as shown in Figure 8 where the configuration cells of the basic building block is as shown in Table 2 The proposed design contains three MV gates: two MV gates are used as AND gates, while the third is used as OR gate. Table 3 compares the proposed design with other QCA designs for the half adder. It shows that the proposed design is more efficient in terms of cell count and with 0.5 clock cycle delay without crossover cells or multi-layers.

Table 3: Comparison between the proposed QCA design for half adder circuit with other designs

Half Adder Logic Structures	Complexity (Cell Count)	Latency (Clock Cycle)
Fig. 9 in [11]	77	1
Fig. 8 in [12]	80	1
Fig. 10 in [10]	64	1
The proposed Design in Figure 8	48	0.5

4 Conclusion

In this paper, the basic building block has been used to implement half adder circuit by adding additional cells and setting the configuration cells. It has been shown that the QCA for half adder that uses the basic building block are more efficient in terms of cell count and/or better clock cycle delay than other proposed designs.

Compliance with ethical standards

The author declare no competing financial interest. The author declare that he has no conflict of interest.

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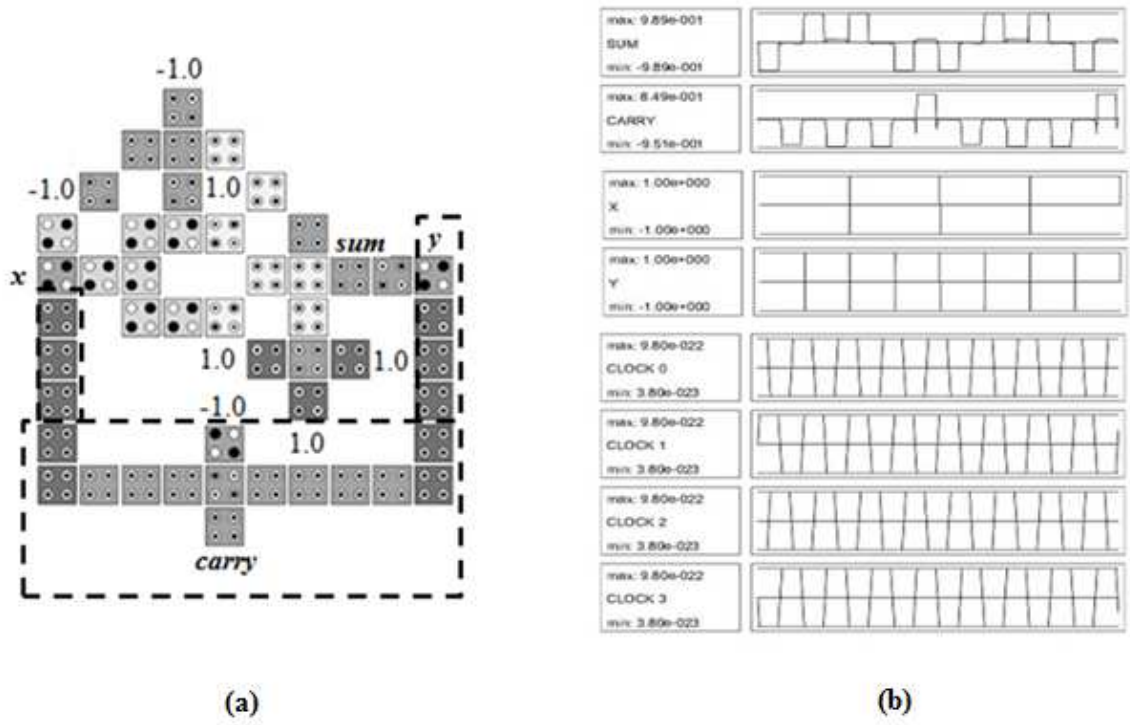

Fig. 8: The proposed QCA for the half adder circuit (a) the layout where the added cells to the basic building block are highlighted with dashed line, (b) the simulation results

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