Applied Mathematics & Information Sciences
An International Journal

http://dx.doi.org/10.18576/amis/110229

Creative Structure of Symmetric and Asymmetric Multilevel Converter Topology Using Single-Double Source Unit

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Received: 21 Dec. 2016, Revised: 17 Jan. 2017, Accepted: 20 Jan. 2017
Published online: 1 Mar. 2017

Abstract: Multilevel converters is the most popular field of research in DC/AC power converters because it has attractive features such as high-quality output voltage, low harmonic content, and low dv/dt stress, and it can be used in medium-voltage, high-power applications such as FACTS devices, which includes the DVR and STATCOM, industrial drives, and renewable energy source-based applications. However, the multilevel converters have the drawback of increasing the number of switches as number of level increases. In order to reduce the power electronic switches, this article proposes a new multilevel converter, which consists of *n* number of isolated DC sources connected in series/parallel to the switches, and its can operate in both symmetric and asymmetric methods. The proposed topology uses a minimum number of the power switches, gate driver circuits, and a less number of maximum blocking voltage switches. To maximize the output voltage level, the cascaded structure of basic unit is proposed. The comparison chart is presented to prove the objective of this article. To demonstrate the performance of the proposed topology, computer simulation using MATLAB/Simulink and prototype-based experimental test were done at 13-level and 31-level output voltage waveforms.

Keywords: Harmonics distortion, multilevel converters, power quality, power switches, symmetric and asymmetric design.

1 Introduction

The multilevel converters have been used in medium-voltage, high-power applications such as industrial motor drives, reactive power compensation, and HVDC. The major advantage of multilevel converter is that it uses medium voltage rating solid state switches (IGBTs), includes low total harmonics distortion (THD), less switching frequency, low electromagnetic interference, absence of filter, reduces the dv/dt or di/dt of switches, and reduces the size and weight problems of conventional transformer-based multipulse converter.

The well-matured multilevel converters are clamped diode, flying capacitor, and cascade H-bridge. The pros and cons of these topologies are well studied in [1–3]. The major disadvantage of these topologies is that the number of levels increases proportionately with the number switches, gate driver circuits, installation area, complex switching pattern techniques and total cost of the converter. Furthermore, the required associated components such as clamping diode and dc-link capacitors are more. This motivates young researchers to research more on multilevel converter, leading to the finding of novel structure, new modulation strategies, and simple control techniques.

However, more than hundreds of novel topologies are present in the literature [4], and these topologies are considerably with reduced switches and gate driver circuits, and different algorithms for the asymmetric configuration are proposed to determine the magnitude of the DC voltage sources. The asymmetric multilevel converter uses a less number of DC sources and switches to generate a higher number of possible output voltage levels, but this is not the case of symmetric converter. Symmetric multilevel converter uses equal magnitude of DC source voltages, which may increase the switches and DC sources, but it offers more redundant states and good modularity.

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Most of the topologies are designed based on the full-bridge converter, which is used to produce both positive and negative voltage levels. However, the full-bridge converter switches should withstand high-voltage ratings, and this increases the cost of the converter. In [5], a new symmetric and asymmetric structure has been proposed, which uses a less number of switches and gate driver circuits compared with the symmetric CHB converter. However, this symmetric topology requires a different voltage rating of switches and high standing voltage on switches.

Moreover, asymmetric topology needs variety of DC voltage sources, which is a drawback. The cascaded transformer is used in the output side to generate increased output voltage waveform in [6]. It offers almost sinusoidal output voltage and increases the transformer efficiency. However, the switches are equal to conventional CHB, and different turn ratio transformers are required, and all the switches should withstand for high voltage, which increases the dv/dt stress, size, and cost of the converter. Switched capacitor-based multilevel converters are proposed in [7].

Using appropriate switching pattern, the capacitors can charge and discharge to produce the stepped output voltage waveform. In this, the number of IGBTs and gate driver circuits needed are more. In [8], a single-phase basic unit is developed based on modified H-bridge converter. In this, different algorithms are proposed to generate maximum possible output voltage waveform with minimum switches. Even more, it uses less DC voltage source and low blocking voltages by switches. It is obvious that required number of varieties of DC sources is increasing as per algorithm 9. Added to this, there are several other topologies proposed with reduction in DC source and IGBTs, which are presented in [9–19].

In these, each topology circuit configuration differs and is proposed with several algorithms to determine the magnitude of DC source voltages. These topologies are optimized for different goals to generate maximum output voltage with minimum IGBTs. Moreover, these topologies require more number of DC sources, variety of DC sources, and high-voltage power switches. This article proposes packed H-bridge-based multilevel converter using single and double source units, which is to minimize the switch count, DC source voltages, and variety of DC source voltage magnitudes. To analyze the performance of proposed topology, it is compared with other well-known recent topologies.

2 The Proposed Topology

The basic single-source (SS) and double-source (DS) units are presented in [20]. The series/parallel combination of switch S_1 and P_1 is connected along with separate DC source voltage as shown in Fig. 1 The switch pair (S_1,P_1) should not be turned on automatically to avoid the short circuit with V_1 and V_2, respectively. The voltage rating of switches for the SS unit is lesser than that of the DS unit. In the double-source unit, the voltages $V_1\}$ and V_2 should be of equal magnitude. The single-and double-source units are connected together to form the generalized structure of multi-stepped dc/dc converter as shown in Fig. 2, and the magnitude of all the DC source should be equal ($V_1 = V_2 = \cdots = V_n = V_{dc}$).

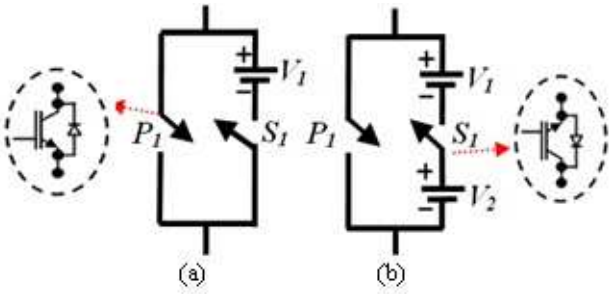


Fig. 1: (a) Single Source Unit (SS Unit) (b) Double Source Unit (DS Unit) presented in [20].

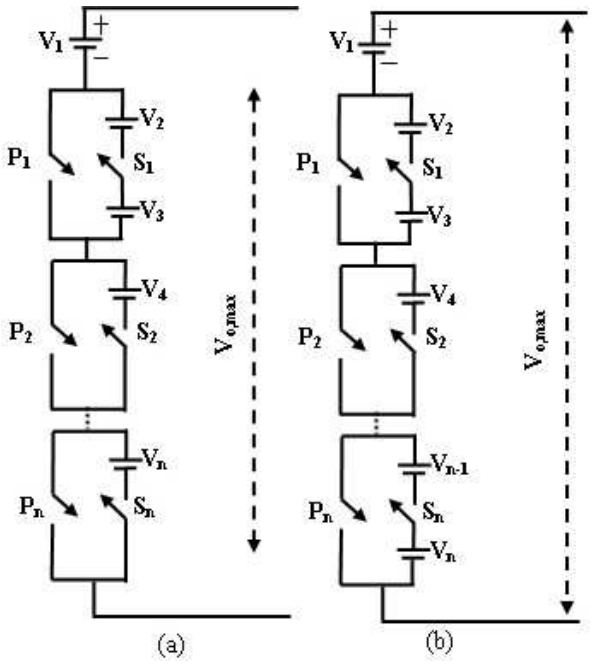


Fig. 2: Generalized structure using SS and DS unit (a) Odd number of sources (b) Even number of sources.

Fig. 2(a) and (b) Generalized structures for both even and odd numbers of DC sources are presented. In order to produce AC output voltage and increase the level of output voltage with reduced number of switches, the SDS

(single-double source) unit is integrated with packed H-bridge unit to form multilevel converter as shown in Fig. 3 and corresponding switching pattern for proposed topology is presented in Table 1. In this article, both symmetric and asymmetric multilevel converters with packed H-bridge are proposed and also the extended topology is discussed.

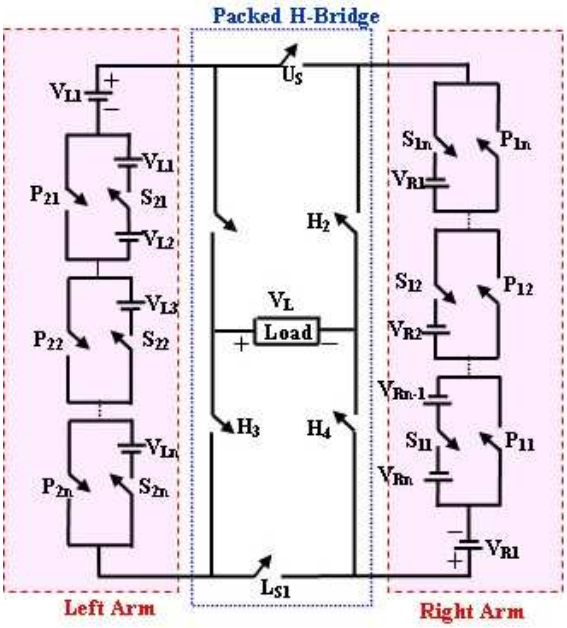


Fig. 3: Generalized structure of proposed multilevel Converter Topology.

The proposed symmetric topology is shown in Fig. 3, which consists of right and left arms along with packed H-bridge unit.

Determination of magnitude DC source voltage for symmetric configuration

The magnitude of DC source voltage for both right and left arms should be symmetrically valued with equal number of DC sources.

$$V_{L1} = V_{L2} = \cdots = V_{Ln} = V_{\mathrm{dc}}$$
$$V_{R1} = V_{R2} = \cdots = V_{Rn} = V_{\mathrm{dc}}.$$

Determination of magnitude DC source voltage for asymmetric configuration

The magnitude of DC source voltage for both right and left arms should be symmetrically valued with unequal number of DC sources.

$$V_{L1} = V_{L2} = \cdots = V_{Ln} = V_{\mathrm{dc}}$$
$$V_{R1} = V_{R2} = \cdots = V_{Rn} = (n+1)V_{\mathrm{dc}}$$

where n is the number of DC sources presented in left arm.

The number of switches (N_{Swicthes}), gate driver circuits (N_{Driver}), the total standing voltage of switches (V_{TSV}), and dc source voltages (N_{Sources}) is calculated as follows:

Number Switches

$$N_{\mathrm{Switches}} = \begin{cases} 2(n+4), & \text{for odd source} \\ 2(n+3), & \text{for even source.} \end{cases}.$$

Number of Levels

$$N_{\mathrm{Level}} = \begin{cases} 4n+1, & \text{for symmetric} \\ 2n(n+2)+1, & \text{for asymmetric} \end{cases}.$$

Number of Sources

$N_{\mathrm{Sources}} = 2n.$

The required number of single-and double-source units for given n number of dc sources is calculated as follows: Since,

$$\left.\begin{array}{l} \mathrm{DS-Unit} = n-3 \\ \mathrm{SS-Unit} = 4 \end{array}\right\} n = \text{odd}$$

$$\left.\begin{array}{l} \mathrm{DS-Unit} = n-2 \\ \mathrm{SS-Unit} = 2 \end{array}\right\} n = \text{even.}$$

Total Standing of voltage of switches

The blocking of switches will be varied in accordance with how they are connected to the source. In this case, the SS unit and DS unit switches should block the V_{1n} and $2V_{1n}$ for right arm and V_{2n} and $2V_{2n}$ for left arm, respectively. The upper (U_{S1} and L_{S1}) and lower switches should withstand the sum of the all the DC sources presented in the converter.

–The single- and double-source units with left and right arm switches:
$2(n-1)(V_{\mathrm{L1}} + V_{\mathrm{R1}})$.

–The packed H-bridge cell right arm switches:
$H_2 = H_4 = nV_{\mathrm{R1}}$.

–The packed H-bridge cell left arm switches:
$H_1 = H_3 = nV_{\mathrm{L1}}$.

–The packed H-bridge cell upper and lower arm switches: $T_{\mathrm{SV}} = (6n^2 + 10n - 4)(V_{\mathrm{dc}})$.

–The packed H-bridge cell upper and lower arm switches:
$U_{S1} = L_{S1} = n(V_{R1} + V_{L1})$.

Table 1: Generalized switching pattern for proposed symmetric topology.

State	S_{11}	S_{12}	$S_{13}\cdots S_{1n}$	S_{21}	$S_{22}\cdots S_{2n}$	H_{S1}	H_{S2}	H_{S3}	H_{S4}	U_{S1}	L_{S1}	Voltage Level ($V_{T,\max}$)
0	–	–	– ⋯ –	–	– ⋯ –	1	1	0	0	0	1	0
	–	–	– ⋯ –	–	– ⋯ –	0	0	1	1	0	1	
1	0	0	0 ⋯ 0	–	– ⋯ –	0	1	1	0	0	1	V_{R1}
2	1	0	0 ⋯ 0	–	– ⋯ –	0	1	1	0	0	1	$V_{R1}+V_{R2}$
3	0	1	0 ⋯ 0	–	– ⋯ –	0	1	1	0	0	1	$V_{R1}+V_{R2}+V_{R3}$
4	1	1	0 ⋯ 0	–	– ⋯ –	0	1	1	0	0	1	$V_{R1}+V_{R2}+V_{R3}+V_{R4}$
5	0	1	1 ⋯ 0	–	– ⋯ –	0	1	1	0	0	1	$V_{R1}+V_{R2}+V_{R3}+V_{R4}+V_{R5}$
6	1	1	1 ⋯ 0	–	– ⋯ –	0	1	1	0	0	1	$V_{R1}+V_{R2}+V_{R3}+V_{R4}+V_{R5}+V_{R6}$
⋮	⋮	⋮	⋮ ⋮ ⋮	⋮	⋮ ⋮ ⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
n	1	1	1 ⋯ 1	0	0 ⋯ 0	0	1	1	0	0	1	$\sum_{i=1}^{n} V_{Ri}$
$n+1$	1	1	1 ⋯ 1	0	0 ⋯ 0	1	1	0	0	0	1	$\sum_{i=1}^{n} V_{Ri}+V_{L1}$
$n+2$	1	1	1 ⋯ 1	1	0 ⋯ 0	1	1	0	0	0	1	$\sum_{i=1}^{n} V_{Ri}+V_{L1}+V_{L2}$
⋮	⋮	⋮	⋮ ⋮ ⋮	⋮	⋮ ⋮ ⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$2n$	1	1	1 ⋯ 1	1	1 ⋯ 1	1	1	0	0	0	1	$\sum_{i=1}^{n} V_{Ri}+\sum_{i=1}^{n} V_{Li}$

–The sum of all the switches is expressed as follows:

$$\text{TSV} = \begin{cases} (12n-4)V_{\text{dc}}, & \text{for symmetric} \\ (6n^2+10n-4)V_{\text{dc}}, & \text{for symmetric.} \end{cases}$$

3 Comparison of the Proposed Multilevel Converter with Other Recent Topologies

Symmetric Topology

To validate the advantages, the proposed topology is compared with other recent topologies, and conventional CHB is discussed. In this section, the different topologies for symmetric configuration are taken into account. The symmetric topology of conventional CHB required $2n+1$ levels and $4n$ IGBTs for n number of DC sources, whereas proposed topology needs $2(n+4)$ for odd DC sources and $2(n+3)$ for even DC sources, respectively. The number of switches in the proposed topology is less than that in the conventional CHB and other topologies as shown in Fig. 4(a). Although the total standing voltage of proposed topology is higher than the conventional CHB topology (Fig. 4(b) the proposed method uses only two switches (upper and lower arm) with maximum blocking voltage, whereas CHB and other topologies require four switches. The number of gate driver circuits is equal to the number of IGBTs in the proposed topology in Fig. 4(c).

Asymmetric Topology

Regarding asymmetric configuration, the required number of switches for different levels and various total standing

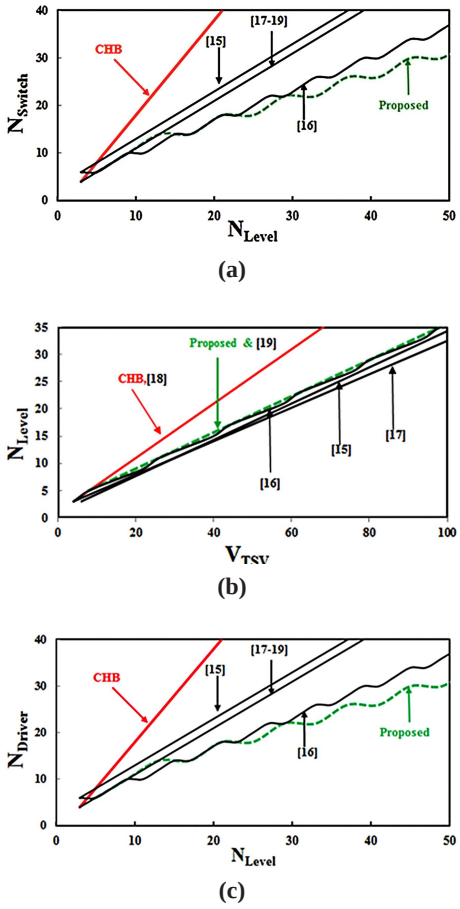
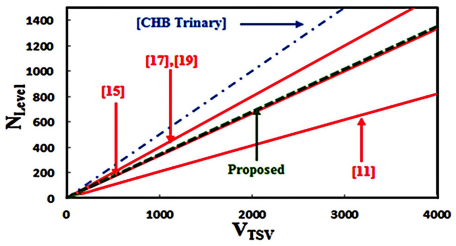
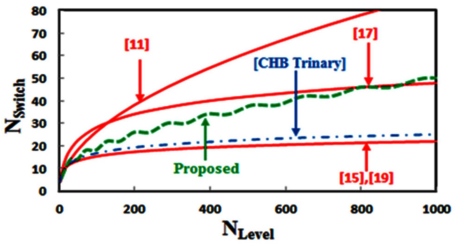


Fig. 4: Comparison of proposed symmetric topology with conventional and other recent topologies (a) N_{Level} vs. N_{Switch} (b) N_{Level} vs. V_{TSV} and (c) N_{Level} vs. N_{Driver}.

voltages against N_{level} is presented in Fig. 5(a) and (b). The different topologies use geometric progression method to generate maximum output voltage level with fewer switches. In the conventional CHB ternary configuration [15] and [19] produce maximum stepped voltage level using fewer switches. The proposed asymmetric method uses less switches compared with [11] and [17] for same output level. However, in order to make the proposed topology more efficient, the cascaded connection of proposed asymmetric converter is presented in the next section.



(a)



(b)

Fig. 5: Comparison of proposed asymmetric topology with conventional and other recent topologies (a) N_{Level} vs. N_{Switch} and (b) N_{Level} vs. V_{TSV}.

4 Proposed Cascaded Asymmetric Multilevel Converter

As said earlier, the proposed asymmetric configuration required large number of switches, gate driver, and higher blocking voltage. In this section, the cascaded connection of proposed asymmetric configuration is presented and it offers low standing voltage, lower number of switches, and higher number of levels with minimum number of DC sources and the variety of DC sources. The *k*th unit switches should withstand maximum blocking voltage.

The generalized structure of the proposed cascaded topology is shown in Fig. 6. In this, left arm, right arm, and upper and lower arm switches require different voltage ratings, and they are discussed as follows:

–The single-and double-source unit left and right arm switches: $2(\text{n}-1)(\text{V}_{\text{L1}}+\text{V}_{\text{R1}})$.

–The packed H-bridge cell right arm switches: $H_2 = H_4 = nV_{\text{R1}}$.

–The packed H-bridge cell left arm switches: $H_1 = H_3 = nV_{\text{L1}}$.

–The packed H-bridge cell upper and lower arm switches: $U_{\text{S1}} = L_{\text{S1}} = n(V_{\text{R1}} + V_{\text{L1}})$.

–The total standing voltage for proposed single unit is: $\text{TSV} = (6\text{n}-2)(\text{V}_{\text{L1}}+\text{V}_{\text{R1}})$.

–The total standing voltage for cascaded structure is expressed as follows: $\text{TSV} = \sum_{i=1}^{k} (6\text{n}_{\text{i}}-2)(\text{V}_{\text{Li}}+\text{V}_{\text{Ri}})$.

The magnitude of DC source voltage to produce a maximum output voltage level is determined for each unit as follows:

First unit:
$V_{L1} = V_{\text{dc}}$.
$V_{R1} = (n1+1)V_{\text{dc}}$.

Second unit:
$V_{\text{L2}} = V_{\text{L1}} + 2n_1(V_{R1} + V_{L1})$.
$V_{R2} = (n_2+1)V_{L2}$.

Third unit:
$V_{\text{L3}} = V_{\text{L1}} + n_2 \sum_{j=1}^{2} (V_{Rj} + V_{Lj})$.
$V_{\text{R3}} = (n_3+1)V_{\text{L3}}$.

For *k*th unit:
$V_{\text{Lk}} = V_{\text{L1}} + n_k - \sum_{j=1}^{k-1} (V_{Rj} + V_{Lj})$.
$V_{\text{Rk}} = (n_k+1)V_{\text{Lk}}$.

The generalized equation for the number of levels (N_{Level}) and maximum output voltage (V_{TMax}) against the DC source is as follows:

$$N_{\text{Levels}} = \prod_{i=1}^{k} \left(2n^2 + 4n + 1\right).$$

The maximum voltage for a single unit is $V_{T,\text{max}} = n(n+2)V_{\text{dc}}$ and total maximum voltage is

$$V_{T,\text{max}} = \prod_{i=1}^{k} (n_i(n_i+2))V_{\text{dc}}.$$

The number of IGBTs and driver circuits is expressed as follows:

$$N_{\text{Switch}} = N_{\text{Driver}} = \begin{cases} 2(n+5)k, & \text{for odd source} \\ 2(n+3)k, & \text{for even source.} \end{cases}$$

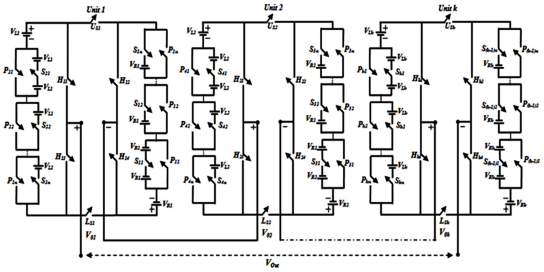


Fig. 6: Generalized structure of proposed cascaded topology.

The number of DC source is $N_{\text{Source}} = 2kn$.

In this comparison, the similar cascaded connection of basic unit is taken into account. The proposed cascaded topology produces maximum output voltage level with lower number of switches and driver circuits as shown in Fig. 7(a) and (b), but in terms of total standing voltage, the CHB trinary configuration has produced the best results with low standing voltage. However, the proposed topology is still placed second compared to other topologies as shown in Fig. 7(c).

5 Power Loss and Efficiency Calculation

There are two major types of well-known losses associated with the IGBT and antiparallel diode: conduction losses and switching losses.

The conduction loss:

This loss depends mainly on the equivalent resistance and on state voltage drop of the IGBT. In order to evaluate the conduction loss, one IGBT is taken into account and remaining IGBT values are multiplied by multiplication factor. The voltage drop of the switches depends on the voltage rating of switches; in this topology, the upper and lower arm switches should withstand higher voltage ratings. The generalized equation to calculate the instantaneous conduction loss for IGBT and diode is expressed as follows:

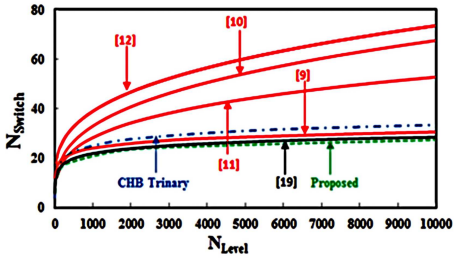
$$P_C, \text{IGBT}(t) = [V_T + R_T i\beta(t)]i(t).$$

V_T, β and R_T represent the on-state voltage drop, a constant that depends on the IGBT (Manufacturing Data sheet), and equivalent resistance of the IGBT.

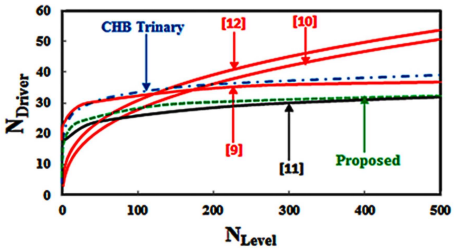
$$P_C, \text{Diode}(t) = [V_D + R_D i(t)]i(t).$$

Total Conduction Loss $(P_{\text{C,T}})$ is

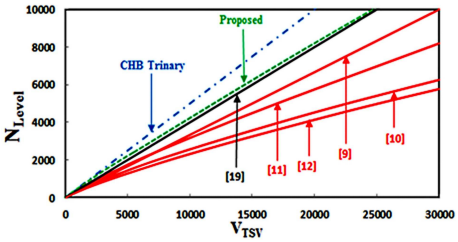
$$P_{C,\text{Total}} = \frac{1}{\pi}\int_0^{\pi}(N_{C,S}(t) \times P_{C,S} + N_{C,D}(t) \times P_{C,D}(t))d(\omega t).$$



(a)



(b)



(c)

Fig. 7: Comparison of proposed cascaded topology with conventional and other recent topologies (a) N_{Switch} vs. N_{Level}, (b) N_{Driver} vs. N_{Level} and (c) N_{Level} vs. V_{TSV}.

V_D and R_D are pointed to the on-state voltage and the equivalent resistance of the diode, respectively. To calculate the conduction losses, it is required to specify the number of existing current path switches $N_{C,S}(t)$ and antiparallel $N_{C,D}(t)$. It is obvious that the proposed topology uses less number of on-state switches.

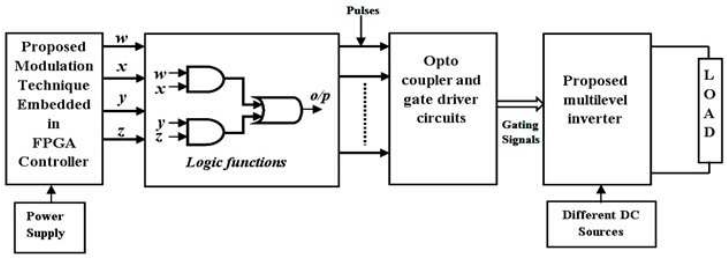


Fig. 9: Functional block diagram of proposed modulation technique.

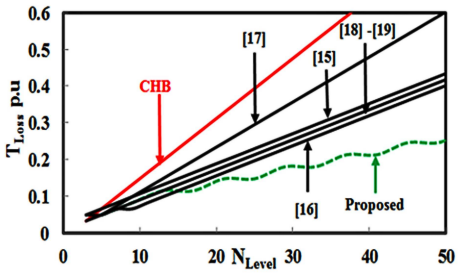
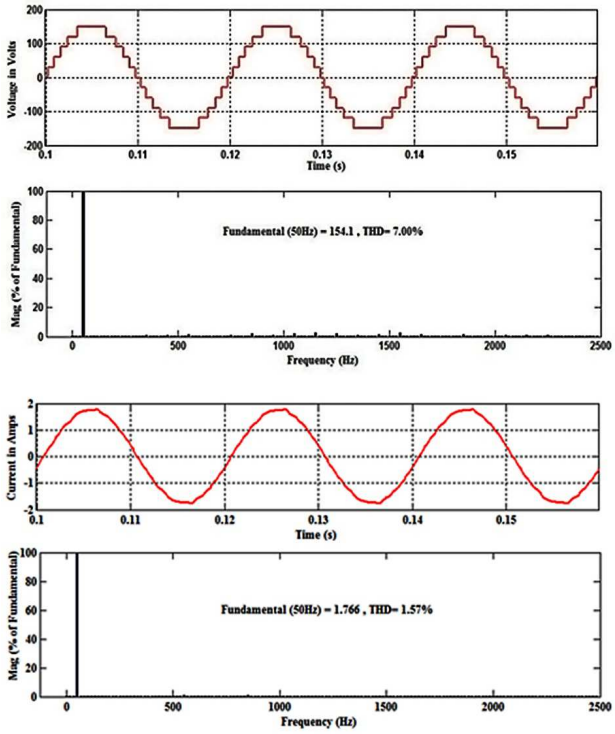
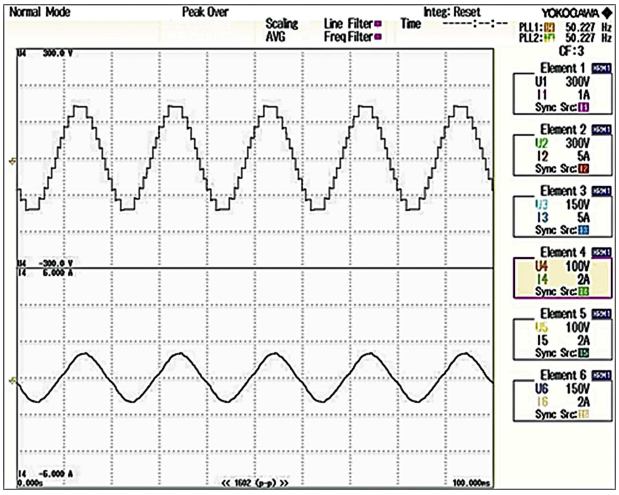


Fig. 8: $T_{\mathrm{LOSS.pu}}$ vs. N_{Level}.





Switching Loss:

The switching loss depends on the corresponding switching frequency. If the fundamental switching frequency is used, it will have low switching losses compared to other non-fundamental switching methods. During turn on and turn off time, the energy losses increase, which may be calculates using voltage across the switches and current.

$$S_{\mathrm{on},j} = \frac{1}{6} V_{\mathrm{sw},n} \times I_{\mathrm{on},n} \times t_{\mathrm{on},n}$$

where $S_{\mathrm{on},j}$, $V_{\mathrm{sw},n}$, $I_{\mathrm{on},n}$, and $t_{\mathrm{on},n}$ represent turn on loss of the nth switch, voltage across the nth switch, current through the nth switch, and turn on time. Similarly, to calculate the turn off losses, the turn on should be replaced with turn off in the above equation as follows.

$$S_{\mathrm{off},j} = \frac{1}{6} V_{\mathrm{sw},n} \times I_{\mathrm{off},n} \times t_{\mathrm{off},n}$$

To find the total switching power losses, they can be expressed as follows:

$$P_{\mathrm{sw,Total}} = 2 f_{\mathrm{fund}} \left[\sum_{n=1}^{N_{\mathrm{Switches}}} \left(\sum_{i=1}^{N_{S_{\mathrm{on}}}} S_{\mathrm{on},ni} + \sum_{i=1}^{N_{S_{\mathrm{off}}}} S_{\mathrm{off},ni} \right) \right]$$

where f_{fund} is the fundamental frequency and $N_{S_{\mathrm{on}}}$ and $N_{S_{\mathrm{off}}}$ is the number of turning on and turning off of the nth switches during half of the fundamental switching

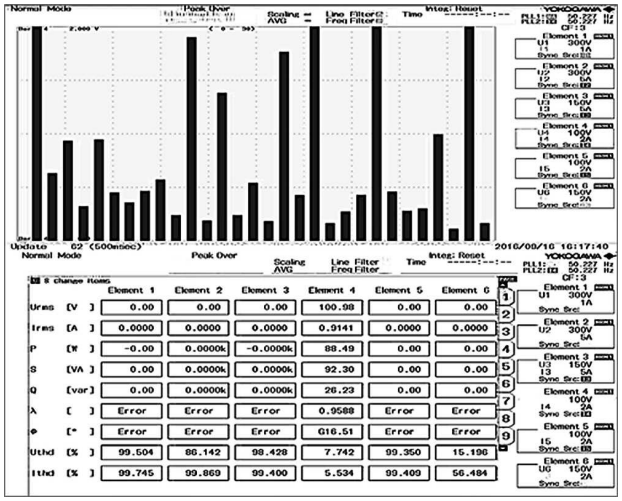


Fig. 10: Proposed 11-level symmetric topology: (a) and (b) Simulation results of voltage and current with FFT spectrum (c) Experimental output voltage and current waveform (d) Voltage FFT with power quality analyzer results(b) and (d) Simulation and experimental Current Waveform.

frequency. Finally, the total power losses (T_{Loss}) of the multilevel converter can be calculated by summing the conduction loss and switching loss as follows:

$$T_{\text{Loss}} = P_{\text{SW,Total}} + P_{\text{C,Total}}$$

Fig. 8 shows the power losses for various levels of proposed topology, compared with other recent topologies. In this comparison, the symmetric topology is taken into account. The switching losses are calculated using conventional SPWM techniques with the switching frequency of 15 kHz. However, in this paper, the fundamental switching technique is implemented in hardware.

Efficiency:

The efficiency of any converter can be evaluated by the following equation:

$$\eta = (P_{\text{out}}/P_{\text{in}}) \times 100.$$

P_{in} is the sum of the output power drawn by the individual DC source, and P_{out} is the output power across the RL load. In this article, fundamental switching (Nearest Level Control) technique is used because the switching and conduction losses are less, which may affect the efficiency of the converter. Tables 2 and 3 show the efficiency of the proposed 11-level symmetric and 31-level asymmetric topologies along with other

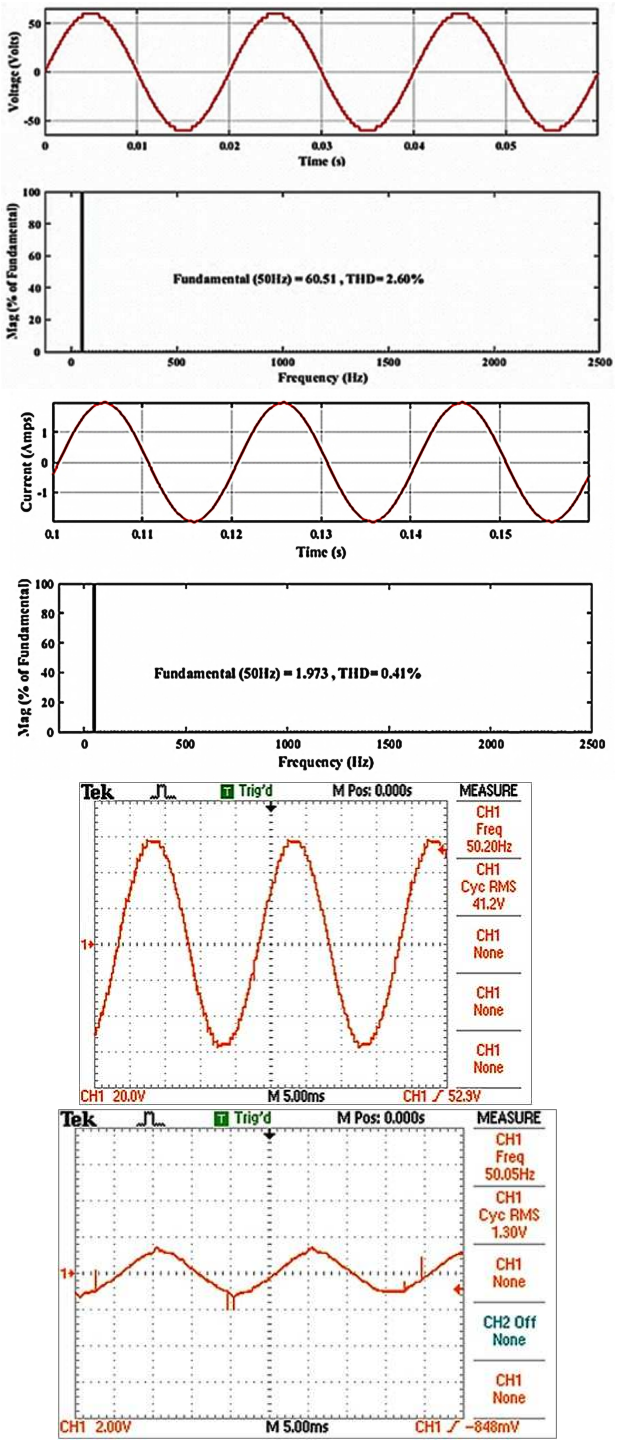


Fig. 11: Proposed 31-level symmetric topology. (a) and (c) Simulation and experimental output voltage waveform (b) and (d) Simulation and experimental current waveform.

Table 2: 11-level symmetric topology: parameters measured for different loads.

Multilevel Converter Configuration	R (Ω)	L (mH)	V_{rms} (V)	I_{rms} (A)	P (W)	Q (Var)	THD %		Efficiency (η%)	$\cos\Phi$
							V	I		
	25	35	77.23	2.82	198.8	87.45	7.33	0.84	91.2	0.915
Proposed	100	100	77.23	0.734	54.01	16.97	7.33	1.10	95.2	0.954
Topology with	100	75	77.23	0.75	56.22	13.25	7.33	1.40	97.07	0.973
Symmetric	100	50	77.23	0.761	57.91	9.096	7.33	1.95	98.5	0.988
Configuration	100	25	77.23	0.768	58.97	4.632	7.33	3.20	99.38	0.997
($V_{\text{dc}} = 21.2$ &	75	100	77.23	0.947	67.3	28.19	7.33	0.87	92.10	0.922
$E_{o,\max} = 106$ V)	50	100	77.23	1.304	85.08	53.46	7.33	0.64	84.4	0.847
	25	100	77.23	1.919	92.02	115.6	7.33	0.44	62.08	0.623

Table 3: 31-level asymmetric topology: parameters measured for different loads.

Multilevel Converter Configuration	R (Ω)	L (mH)	V_{rms} (V)	I_{rms} (A)	P (W)	Q (Var)	THD %		Efficiency (η%)	$\cos\Phi$
							V	I		
Proposed	30	20	42.8	1.396	58.44	12.24	2.60	0.41	97.8	0.979
Topology with	100	100	42.8	0.408	16.66	5.234	2.60	0.35	95.35	0.954
Asymmetric	100	75	42.8	0.416	17.34	4.086	2.60	0.42	97.24	0.973
Configuration	100	50	42.8	0.422	17.87	2.806	2.60	0.51	98.77	0.988
($V_{R1} = V_{R2}$	100	25	42.8	0.426	18.19	1.429	2.60	0.61	99.64	0.997
$= V_{R3} = 16$ V,	75	100	42.8	0.526	20.76	8.698	2.60	0.29	92.17	0.922
$V_{L1} = V_{L2}$	50	100	42.8	0.724	26.25	16.49	2.60	0.23	84.65	0.847
$= V_{L3} = 4$ V)	25	100	42.8	1.066	28.39	35.67	2.60	0.16	62.22	0.623

Fig. 12: Prototype model of experimental setup.

measured parameters such as V_{rms}, I_{rms}, real power (P), reactive power (Q), THD, and power factor $(\cos\Phi)$ for various loads.

6 Simulation and Experimental Results

Prototype hardware model functional block diagram is shown in Fig. 9 The control fundamental switching technique is implemented using an FPGA Spartan XE3S250E controller. These circuits consist of an opto-isolator (for isolation between switch and FPGA controller), a Schmitt trigger (used to converter analog signal to digital pulses), and a buffer. Opto-isolators can work in a wide range of input signal pulse widths, but a separate isolated power supply is required for each switching device. For isolation, either pulse transformer or opto-isolators can be used. The opto-isolator-based drivers are used in this prototype model.

Symmetric Topology:

Fig. 10(a)–(d) shows an 11-level output voltage and current of proposed topology for both simulation and experimental results, respectively. In this topology, the values of DC sources are equal, and each has the value of 21.2 V. The THD values of output voltage and current based on simulation are 5.82% and 1.34% and on experimental are 7.51% and 1.1% respectively. To implement the 11-Level proposed converter, 5 DC voltage sources, 10 IGBTs (BUP400D) and 10 IGBT drivers (HCPL316j) are used. In both simulation and experimental, the same parameters such as magnitude of DC source and load values are used. It is worth to mention here that as the number of levels increases, both voltage and current THDs decreases using fundamental switching techniques. The high inductive load is used, which acts as a filter in load and current becomes close to sinusoidal waveform. Table 4 shows the voltage and current ratings of the hardware prototype model.

Table 4: Simulation and experimental parameters for symmetric topology.

S.No.	Description	Ratings
1.	RL Load Values	$R = 85$ Ohm and $L = 65$ mH
2.	IGBTs Model No: BUP400D	$V_{CE} = 600$ V and $I_C = 22$ A
3.	Gate Driver Circuits: HCPL316j	Drive upto $I_C = 150$ A and $V_{CE} = 1200$ V
4.	Pulse Generator	FPGA Spartan XE3S250E
5.	$V_{L1} = V_{L2} = V_{R1} = V_{R2} = V_{R3} = 30$ V	$V_{\text{out}} = \pm 150$ V, $V_{\text{rms}} = 100.23$ V

Table 5: Simulation and experimental parameters for asymmetric topology.

S.No.	Description	Ratings
1.	RL Load Values	$R = 30$ Ohm and $L = 20$ mH
2.	IGBTs Model No: BUP400D	$V_{CE} = 600$ V and $I_C = 22$ A
3.	Gate Driver Circuits: HCPL316j	Drive upto $I_C = 150$ A and $V_{CE} = 1200$ V
4.	Pulse Generator	FPGA Spartan XE3S250E
5.	$V_{L1} = V_{L2} = V_{L3} = 4$ V, $V_{R1} = V_{R2} = V_{R3} = 16$ V	$V_{\text{out}} = \pm 60$ V, $V_{\text{rms}} = 41.2$ V

Asymmetric Topology:

In asymmetric topology the values of dc sources are not equal. Right arm sources have the value of $V_{R1} = V_{R2} = V_{R3} = 16$ V and Left arm source values are $V_{L1} = V_{L2} = V_{L3} = 4$ V, which can generate a possible output voltage of 31-Level. The right arm switches always have maximum blocking voltage compared to other side switches. However, the maximum blocking voltage switches of proposed topology is upper arm and lower arm switches and the maximum blocking is 60V. The experimental THD of voltage and current is 2.84% and 0.73% respectively, which is very close to the simulation THD as shown in Fig. 11(a)–(d) and the details of experimental values listed in Table 5. The prototype model of the experimental setup is shown in Fig. 12.

7 Conclusion

A new packed H-bridge multilevel converter is introduced in this article, and this is configured in both symmetric and asymmetric configurations. The symmetric configuration produces $2n+1$ level with minimum switches, but the proposed asymmetric configuration requires a large number of switches. For asymmetric configuration, the new cascaded structure has been proposed, which is based on the series (cascaded) connection of the submodule of the packed H-bridge. The recommended cascaded structure has a flexibility to extend up to k units and determined the magnitude of DC sources to generate the highest number of output voltage levels.

The cascaded structure has been selected and optimized for maximum number of output voltage levels for minimum number of IGBTs, gate driver circuits, total standing voltage, and reduced DC sources. To confirm the advantages of the proposed topology is compared with other recent topologies with different parameters such as N_{level} vs. N_{Switch}, N_{Driver} vs. N_{Switch} and total standing voltages. It is shown that the proposed topology not only has lower number of power electronic components, but also the packed H-bridge unit that operates at a low standing voltage and it uses less number of maximum blocking voltage switches (upper and lower arm switches). This extends the applications of the recommended converter is more suitable for medium voltage high-power applications.

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